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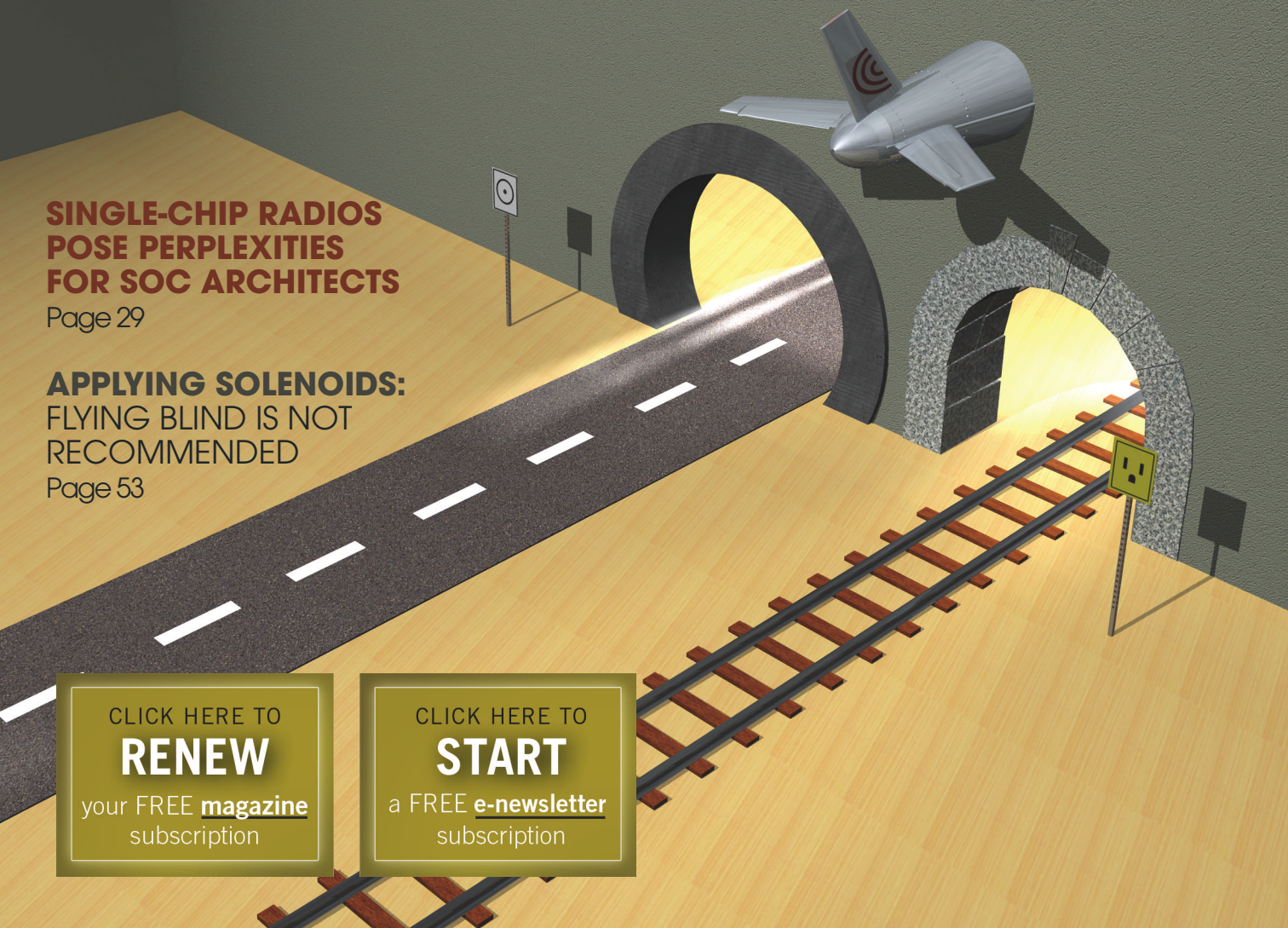
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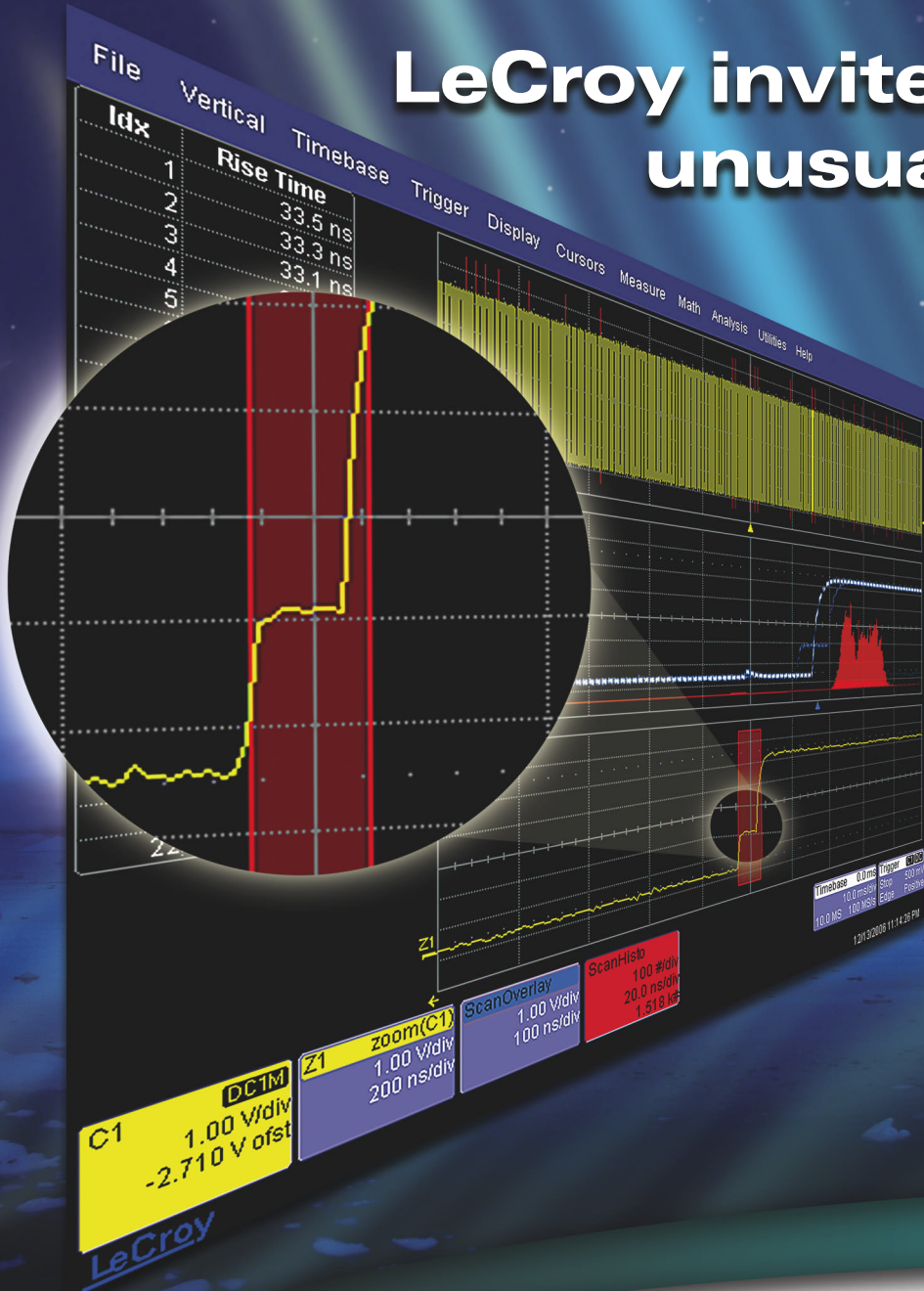
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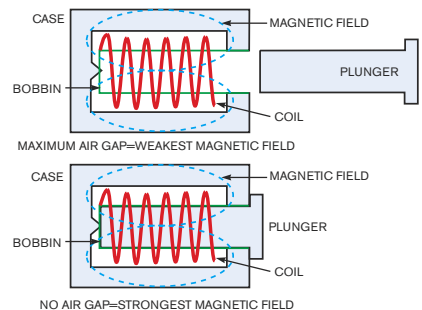
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Applying solenoids: Flying blind is not recommended

53 Solenoids—especially in applications that require them to rapidly energize and de-energize—require an understanding of their operational subtleties and your control-circuit options.

by Timothy G Morrill,
Raytheon Co



EDN HANDS-ON PROJECT Home transportation: benchmarking power line, 802.11, and Ethernet

40 Home networks carrying high-definition video and other large-data payloads need ample bandwidth and consistent performance. Can power-line technology fit the bill for long distances, or must consumers resign themselves to stringing Category 5 cable? And which 802.11 standard will suffice for shorter distances?

by Brian Dipert,
Senior Technical Editor

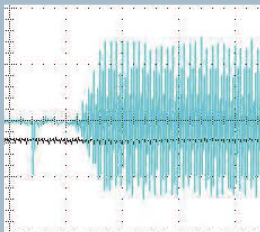


Single-chip radios pose perplexities for SOC architects

29 Integrating wireless capability into an SOC requires careful attention to partitioning and architectural decisions that often have no clear-cut answers.

by Ron Wilson, Executive Editor

DESIGN IDEAS



65 Simple and effective inrush-current limiter stops surges

68 Inverting sample-and-hold amplifier requires no external resistors

70 Single IC forms inexpensive inductance tester

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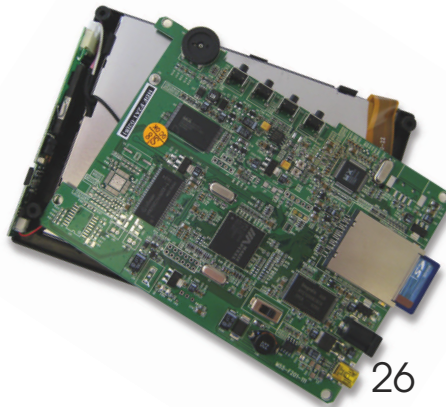
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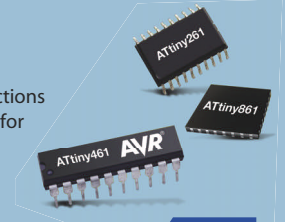
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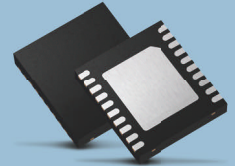
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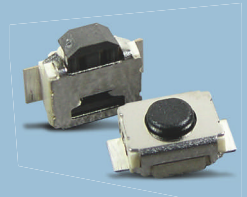
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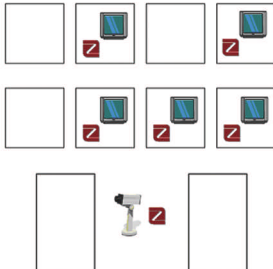
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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Research confirms suspicions and reveals surprises

Here at *EDN*, we carry out several major research projects every year. We use the research to make decisions about what we cover and how we provide information to you—the reader and Web-site visitor. Every 18 to 24 months, we repeat a project called “Mind of the Engineer.” The project looks at a mix of what our readers are working on, the pressures of the job, the prevalent enabling technologies,

engineering disciplinary skills, and information resources and Internet usage. The full survey is massive, but I’ll present a few excerpts here and perhaps more in future columns.

As always, the “Mind of the Engineer” produced both expected and surprising results. We conducted the research in North America, Europe, Japan, China, and a Pan-Asian region that includes Taiwan, Korea, Singapore, and Hong Kong. The number of respondents varied from 121 in Europe to more than 1100 in North America.

Interest in analog design is the first item that jumped out at me as I reviewed the data. We asked participants to select the engineering disciplines with which they’re involved. The participants could select more than one discipline. In every region except Asia, analog design was the top choice. In North America, Europe, and Japan, analog garnered 53, 56, and 54% of the vote, respectively. In China the analog response totaled only 36%, but that percentage was still the top response. In Asia, the percentage was 34%—barely losing out to processor-based design at 36%.

In general, board-based system de-

In all regions, respondents noted increasing workloads and the demand to accelerate the design cycle to rush products to market.

sign was the second vote getter. Power-systems design, a close cousin to analog, came in third, followed by processor-based design. Only in China did IC design top 20%. In the rest of the regions, the numbers for IC design were in the teens. Clearly, China has become a major player in design in general and in IC design specifically.

We also asked participants how their work has changed compared with three years ago. The No. 1 answer in North America, Europe, and China was “working with a broader set of software tools.” Moreover, one response noted that while tools make it easier to work with advancing technology, the tools also have a huge learning curve. In Japan and Asia, respondents cited “the need to make

technology choices faster” as the biggest change, and that response appeared in the second position in the other regions.

Not surprisingly, North American respondents named “keeping up with the latest technologies” as their biggest issue. But some of the other responses are quite interesting. In Japan, a respondent noted a problem with declining academic standards in engineering programs. I can only speculate that the comment stems from the increasing number of students in engineering programs.

In all regions, respondents noted increasing workloads and the demand to accelerate the design cycle to rush products to market. A North American respondent noted, “The time-to-market pressures have increased dramatically. It makes it very difficult to design and build quality products with such short design cycles.” And a Japanese respondent noted quality problems associated with working with engineers in other regions.

For me, the best question came at the end of the survey. We asked respondents whether they would recommend the engineering profession to a student. In all regions except China, the positive response topped 80%, with Europe coming in at 89%. Chinese respondents voted 70% affirmatively. In recent years, both research and my intuition have indicated declining satisfaction with the engineering profession. I’ve never quite understood why. I think it’s about the most exciting choice a student can make, and I’m certainly encouraging my son to pursue an engineering path. I’m happy to see the upward trend.**EDN**

Contact me at mwright@edn.com.

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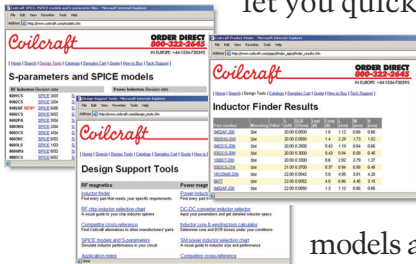


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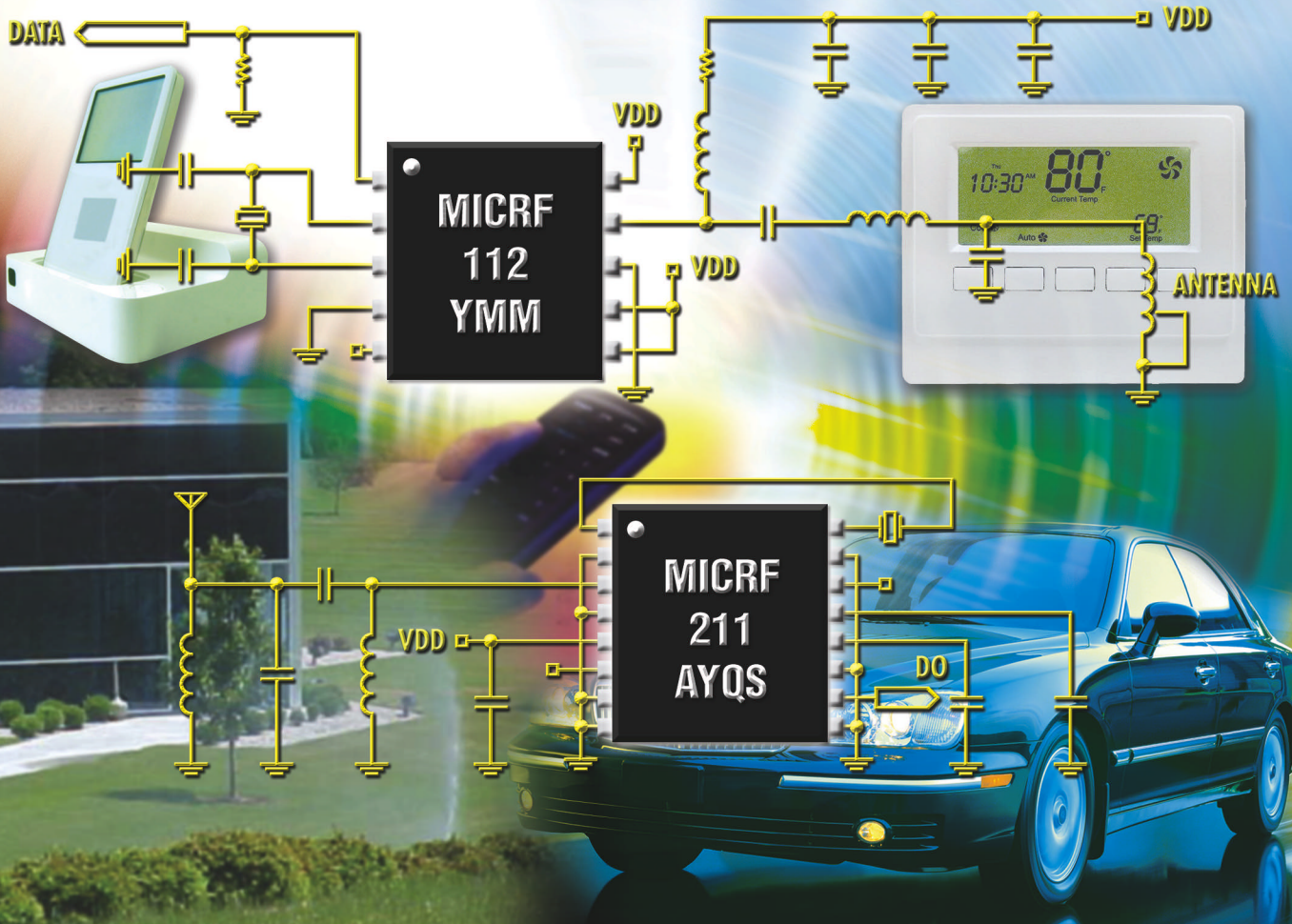
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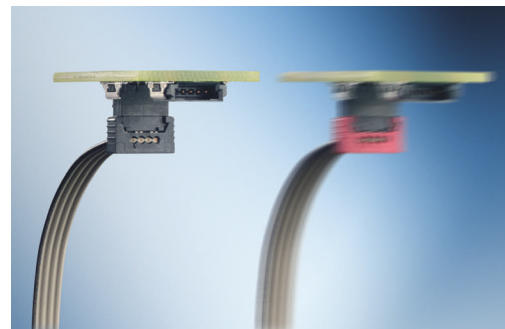
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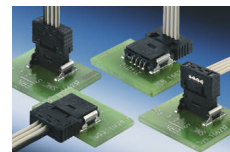
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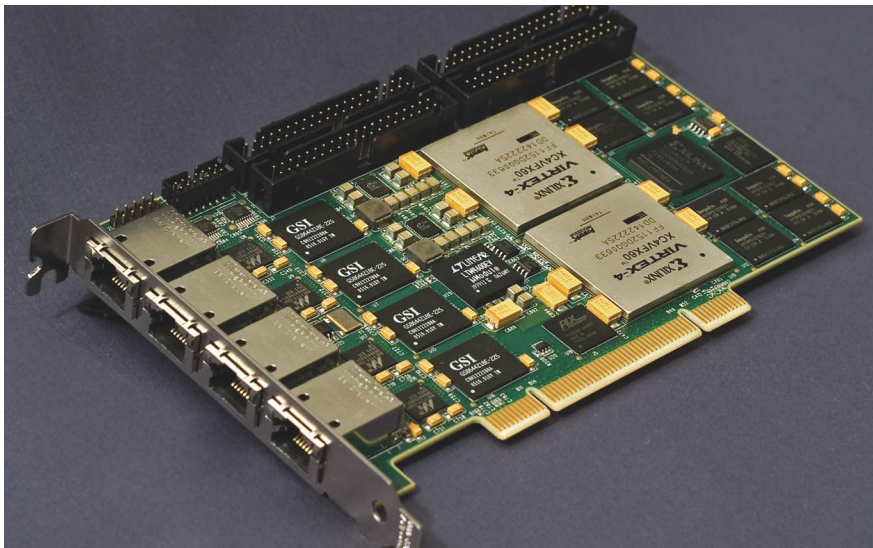
FPGA board suits streaming-communications applications

Targeting high-performance streaming-system applications, such as telecommunications-protocol analysis, software-defined radio, and real-time-video processing, Embedded Systems Design recently announced the StreamBlade SOE-4 short-form PCI card featuring two Xilinx (www.xilinx.com) Virtex-4 FX60 FPGAs or two Virtex-4 FX100 FPGAs. The SOE-4 implements Ethernet as a distributed-computer backplane, and the PCI bus handles only power, configuration, and control. The SOE-4 supports four independent GbE (gigabit-Ethernet) ports plus four ATA connectors, which provide for direct user-configurable access to both FPGAs. With two 8-Mbyte banks of zero-bus-turnaround

SRAM and two 128-Mbyte banks of SDRAM per FPGA, developers can use the SOE-4 as a quad PowerPC 405 processing board, as a pure-FPGA-processing board, or for combined hardware/software-boundary processing. The board comes with a development kit that includes sample applications, FPGA reference designs, Linux PCI device drivers, and host utilities for loading FPGA bit streams and executable files into flash memory. With two Xilinx Virtex-4 FX60 FPGAs, the StreamBlade SOE-4 costs \$6800 (one). Delivery is eight weeks after receipt of order.

—by Warren Webb

▶ **Embedded Systems Design Inc.**, www.embedded-sys.com.



The new StreamBlade SOE-4 PCI board delivers dual FPGAs to process real-time streaming data for telecom and software-defined-radio applications.

FREE WIRELESS-DESIGN TOOL TARGETS SHORT-RANGE RADIOS

A variety of applications—ranging from wireless-power-meter reading to security to factory control—relies on short-range radios. Analog Devices is now offering a free design-and-simulation tool for such applications. The SRD (Short Range Device) Design Studio speeds product development and allows you to view simulations in the time and the frequency domains. The product works with the company's ADF70xx family of short-range transmitters and transceivers. You can download the tool at www.analog.com/srddesign.

—by Maury Wright

▶ **Analog Devices**, www.analog.com.

FEEDBACK LOOP

“It’s good to see engineers account for switching losses in capacitors, but too often they’re foolin’ themselves ...”

—Reader Cecil Deisch tells you why, in *EDN’s* Feedback Loop, at www.edn.com/article/CA6437957. Add your comments.

ChipVision's Orinoco II generates RTL for low-power design

Privately held EDA company ChipVision has extended the features of its Orinoco ESL (electronic-system-level) IC-architecture-estimation tool so that it now has both design- and power-estimation capabilities. Previously, the tool boasted features only for analyzing the power consumption of ICs at the ESL. Orinoco II can now help designers generate low-power RTL (register-transfer-level) code.

Until now, a lack of front-end power tools has forced design teams to deal with low-power design mainly during the gate level and physical-design steps, according to company president Thomas Blaesi. At that point, designers can make only a limited number of adjustments to their designs to lower their designs' power.

"Most industry experts agree that the best method for effective power reduction is at the system level," Blaesi says. "Selecting the correct architecture can make a huge impact on power savings—roughly 80% of power savings can be gained by creating a good architecture."

To help engineers gain that advantage, the company has created new technology for Orinoco that allows system

Once you load the source code into the tool, the tool generates a tree-implementation profile or an activity profile. The tool then performs an interactive synthesis that allows users to make power, timing, and area trade-offs.

and RTL designers to interactively optimize area, power, and timing constraints to create RTL code. "We've created a technology that allows system and RTL designers to execute many architectural explorations and select the one with the lowest power consumption that still meets timing and area budgets," says Blaesi.

Users feed the tool a C, C++, or SystemC version of their designs as well as IP (intellectual-property) blocks. They then feed the tool power

constraints, such as clock-gating, clock-infrastructure, and power-supply information in either the UPF (Unified Power Format) or the CPF (Common Power Format). Users also feed the tools Synopsys .lib files, which, among other data, provide Orinoco II with transistor-leakage estimates.

You need to run the flow once per targeted process technology, says Blaesi. During that run, Orinoco II creates the power libraries that the tool uses. "The flow is automated, so customers can run it, or a ChipVision engineer can do it for them," he says. Once you load the source code into the tool, the tool generates a tree-implementation profile or an activity profile for the design. The tool then performs an interactive synthesis that allows users to make power, timing, and area trade-offs. Users generate versions of the architecture and then select the one that best meets their power, timing, and area budgets. Once they choose an architecture, they use Orinoco II to generate RTL and create synthesizable Verilog. "At this stage, the RTL-design team can begin the engineering-change process and modify the code as desired," says Blaesi. "We still believe the

PROCESSOR SUPPORTS SECURITY, ENCRYPTION, AND COMPRESSION

Hifn has announced the 4450 FlowThrough security processor—the latest addition to a family of such processors. The 4450 targets systems that must compress data in real time, apply security protocols, handle encryption algorithms, or perform all of these tasks. The IC supports the IPsec (Internet Protocol security) standard, and the company claims that the device handles functions that now typically require three separate ICs. The IC will find use in storage networks, fabrics, and other data-center applications; it sells for \$80 (OEM volumes).

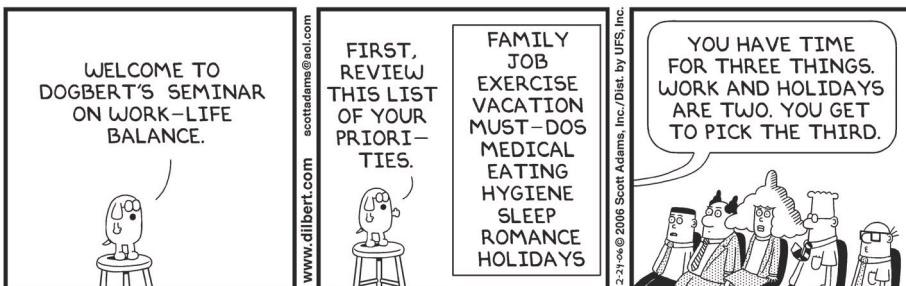
—by Maury Wright
 ▶ Hifn, www.hifn.com.

RTL is going to be the golden model for some time, so we make sure the RTL we generate is human-readable."

Using the tool, beta customers have reduced power in their designs by 30 to 40%, reduced development times by a factor of 60, and realized a ninefold decrease in the amount of code necessary for achieving a low-power design. The company expects to release the tool this year and demonstrated it at the Design Automation Conference in San Diego in June. The company has not yet determined a price for the tool.

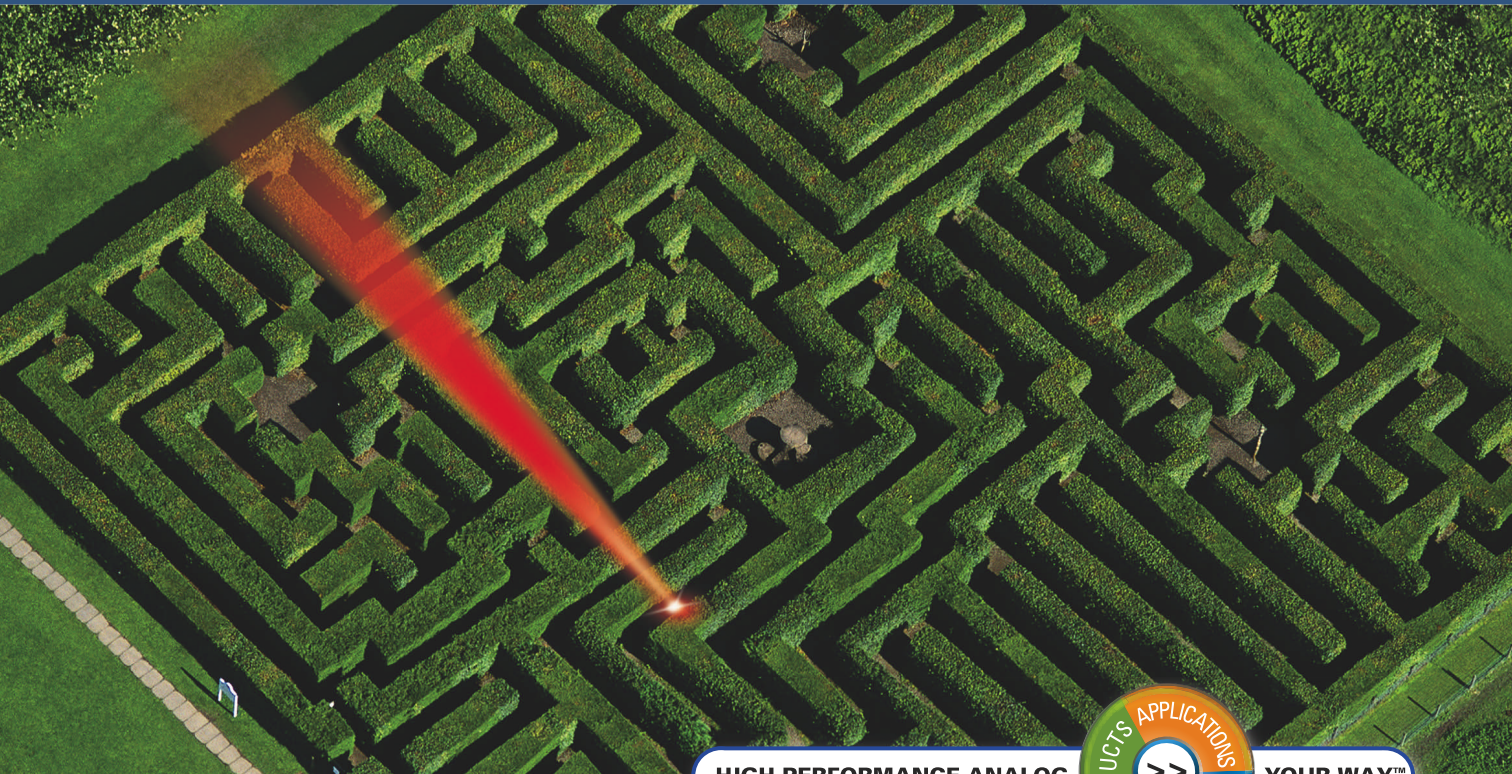
—by Michael Santarini
 ▶ ChipVision, www.chipvision.com.

DILBERT By Scott Adams

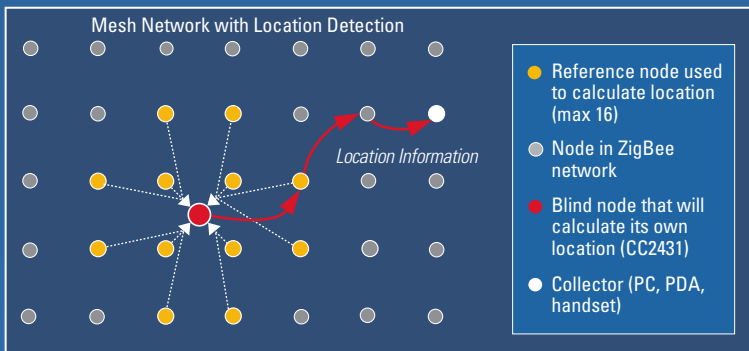


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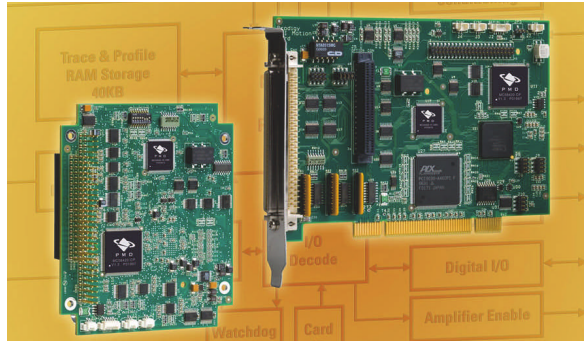
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Motion-control card targets PCI, PC-104, and CAN bus

The new Prodigy motion-control cards from Performance Motion Devices can drive as many as four brushless, stepper, and dc motors. The cards allow for user-selected profiles, including electronic gearing of two-axis, S-curve, trapezoidal, and other trajectories. They use the host PC only to provide power and to communicate the motion profiles through the CAN (controller-area-network) bus, PCI, PC-104/ISA, or serial port, ensuring that the motion-control system is not at risk due to the long latencies and unpredictable operation of the operating system. The card provides a feedforward PID (proportional/integral/differential) filter and dual bi-quadratic filters. Outputs of the cards include PWM, analog, pulse, and direction.

The cards can trace as many as four motion-parameter registers, including those for position, velocity, acceleration, and servo lag. You can stream the



The Prodigy motion-control cards provide servo-loop rates as great as 50 μ sec/axis, quadrature-encoder-input rates of 8 million counts/sec, and pulse- and direction-output rates of as many as 5 million pulses/sec.

trace data to the host or store it on the card for later examination. The ability to trace the motion registers enables you to deduce optimum trajectories and perform servo-tuning. Further, you can use the error values in adaptive-machining applications in which a card records the motion deviation from ideal on the first manufactured part. An engineer or an adaptive program can then correct for any deviations in the control program, so that subsequent

parts are more accurate, even when the tool loads change due to repeatable breakouts or other problems.

The position range of the card is ± 2 billion counts, and the signal-conditioned quadrature-encoder inputs reject noise. Available in both short-PCI-card and ISA PC-104 formats, the cards sell for \$380 (OEM quantities).

—by Paul Rako

► **Performance Motion Devices Inc.**, www.pmdcorp.com.

FEEDBACK LOOP

“A lot of people seem to be working on ‘superbatteries’ on the theory that we’ll need something to even out the variability of wind and solar, but the answer is staring us in the face. ... Pumped-storage hydroelectric power ... can be located virtually anywhere there are sizable hills—or even big, deep holes in the ground.”

—Reader Alden Wilner, in *EDN's Feedback Loop*. Read more about wind, solar, and other power sources and add your comments at www.edn.com/article/CA6399098.

Integrated Hall-effect sensors shrink position sensors and motor drivers

Fine-pitch-detection applications incorporating encoder-ring magnets require precise alignment of their location sensors. With that requirement in mind, Allegro Microsystems recently introduced the A3423 dual-channel direction-detection sensor. The device has two Hall-effect elements that are photolithographically aligned to more than 1 micron to ensure sensitivity and temperature stability in harsh automotive and indus-

trial environments. The device offers short-circuit-protected speed and direction outputs, and its input operating voltage ranges from 3.8 to 24V. The A3423 is available in a four-pin SIP, and a plastic, eight-pin, SOIC surface-mount package is in development. It sells for \$1.78 (1000); leadtime is 14 weeks.

The company also introduced the A1442 full-bridge motor driver for low-voltage, bipolar, brushless-dc motors,



The A3423 incorporates two Hall-effect elements to sense both the speed and the direction of encoder-ring magnets.

which often act as vibration motors in cellular phones, pagers, electronic toothbrushes, handheld-video-game control-

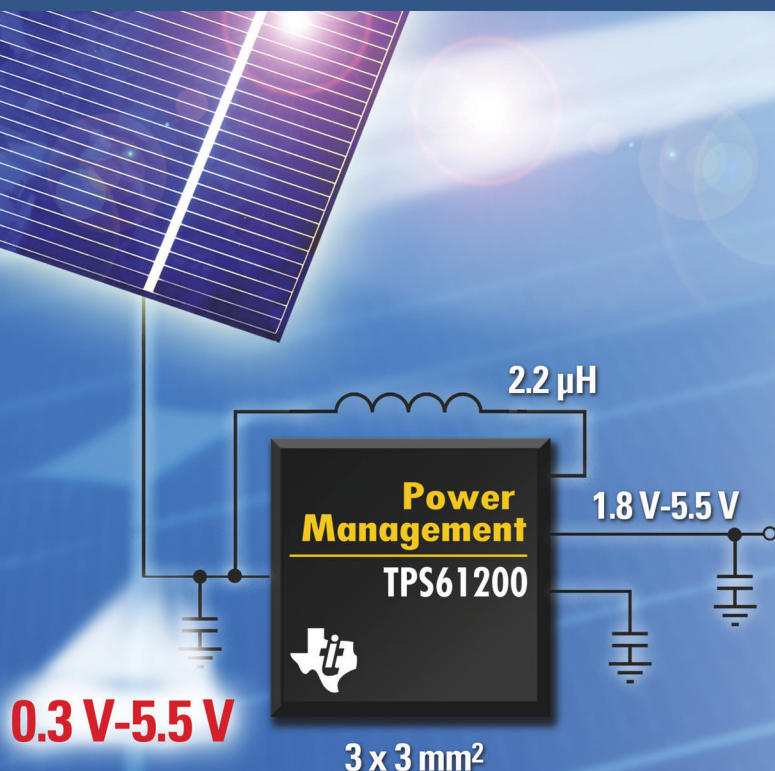
lers, and low-power fans. The 1442's Hall-effect sensor provides motor commutation by detecting the rotational position of an alternating-pole ring magnet. The device comes with the Hall-effect sensor, the motor-control circuitry, and the full-output bridge. The input voltage goes as low as 1.8V and includes reverse-battery and output-short-circuit protection. The six-pin MLP/DFN package measures 1.5 \times 2 \times 0.4 mm and sells for 39 cents (1000); leadtime is six to eight weeks.

—by Margery Conner

► **Allegro Microsystems**, www.allegromicro.com.

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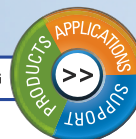
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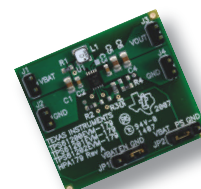


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TPS61081	2.5 to 6.0	1.3	V_{IN} to 27	85	3 x 3 mm QFN-10	\$1.65
TPS63000	1.8 to 5.5	1.8	1.2 to 5.5	96	3 x 3 mm QFN-10	\$2.75
TPS717xx	2.5 to 6.5	–	0.9 to 6.2	–	1.5 x 1.5 mm SON	\$0.40

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 **TEXAS INSTRUMENTS**

Test tool for new automotive bus hides inside scope

LeCroy Corp has added an integrated oscilloscope-based test tool for the new 10-Mbps FlexRay automotive bus to its broad array of automotive- and embedded-system test and debugging tools. The new tool, which also supports forthcoming 2.5-, 5-, and 20-Mbps versions of FlexRay, fully integrates the trigger hardware within the company's WaveRunner Xi small-footprint, large-screen digital scopes; correlates physical-layer signals with protocol-layer data in one display; and provides what the company calls the most complete FlexRay triggering and decoding capabilities available in a scope.

The FlexRay trigger isolates static and dynamic slot IDs, cycle-count numbers, frame qualifiers, and symbols, and the decoder superimposes a color-coded overlay on the



The FlexRay triggering and decoding capability provides a single display that makes evident how the physical layer's behavior manifests itself in the data and control signals that traverse the bus.

physical-layer waveform. Because the trigger is not a node on the FlexRay network, it requires no network reprogramming. You merely connect a differential probe to the bus and capture data. A straightforward touchscreen-display-based user interface provides

access to all protocol triggers. As do LeCroy's other serial-data-debugging tools, the new tool allows conditional triggering on in-range, out-of-range, less-than, or greater-than conditions, permitting triggering on a range of slot IDs or cycle numbers.

The WaveRunner Xi scopes provide additional measurement capabilities that can be useful to FlexRay chip and system designers who need to perform physical-layer compliance tests but who find that no other single tool will perform all of the tests. With its extensive math and measurement capabilities, the WaveRunner enables designers to perform pass/fail mask testing and timing measurements on physical-layer signals to establish FlexRay compliance. Mixed-signal options allow users to add as many as 36 logic-timing-analysis channels to the scopes.

The FlexRay triggering and decoding capability is available as an option to WaveRunner Xi oscilloscopes for a US list price of \$3995.

—by Dan Strassberg

► **LeCroy Corp.**, www.lecroy.com.

Linear introduces surface-mount low-dropout regulator

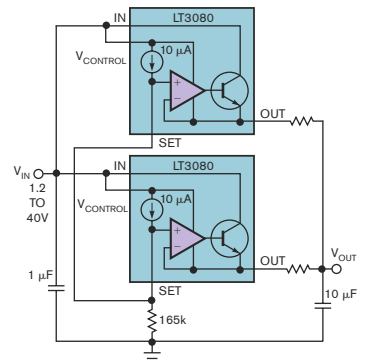
The new LT3080 adjustable linear regulator from Linear Technology Corp has only a 1-mV offset between the voltage on the adjust pin and the output voltage, meaning that only 10 mΩ of PCB (printed-circuit-board)-trace resistance in the output path balances the currents among paralleled devices. The device's set pin outputs a fixed 10-μA current that reacts against a resistor to create a fixed voltage. With only 10-mΩ trace resistance from your PCB that serves as emitter degeneration, the parts all share current. Maximum input voltage is 40V. The unit has separate pins for the NPN-pass-transis-

tor collector and the power for the internal-chip circuitry. This feature allows the internal chip to operate from a higher voltage, so that you can drive the pass transistor to full saturation and provide a 300-mV dropout. If you can live with the normal dropout of a non-PNP part, you can also run the part with both pins wired together.

"This is the first change in architecture for linear regulators since the introduction of the three-terminal adjustable [regulator]," says Bob Dobkin, vice president of Linear and inventor of the new part. He points out that conventional linear regulators do not adjust the output to less than 1.2V. In con-

trast, the LT3080 adjusts down to 0V simply by using a low-value resistor. Another shortcoming of conventional regulators is that they are difficult to connect in parallel because a voltage sets the regulators, and the internal reference is not tightly controlled. You therefore must use significant ballasting resistors in the outputs of the paralleled devices to ensure that they share current. The LT3080 also has lower quiescent current than older linear regulators.

The LT3080 is available now and comes in eight-lead, 3×3-mm DFN packages; thermally enhanced MSOPs; five-lead TO-220 packages; and SOT-



The LT3080 uses a fixed set-pin current to allow designers to connect several devices in parallel. This feature makes the part ideal for use in surface-mount systems in which any IC has only 1.1W output.

223 packages. Prices start at \$1.81 (1000).—by Paul Rako
► **Linear Technology Corp.**, www.linear.com.

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The AD9549 is a two input clock generator with extended holdover functionality. It has a programmable loop filter to clean jitter from input clocks and features flexible output frequency options. In addition, automatic redundant reference clock switchover with user-selectable rate of phase adjustment helps ensure system stability and maximizes network uptime.

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VOICES

VSIA President Kathy Werner on closing down an industry consortium

Industry consortia are mostly, like diamonds, forever. Kathy Werner is president of the VSIA (Virtual Socket Interface Alliance), an industry consortium devoted to streamlining the selection and transport of semiconductor IP (intellectual property). She is also IP manager at Freescale Semiconductor. *EDN* recently asked her why VSIA elected to shut itself down.

Why would a thriving industry organization like the VSIA vote to shut itself down?

A It's not an easy decision. But the board feels that this is the best thing for the industry and for the work we have done. VSIA has pioneered a number of important tools for the IP industry. But there are, if anything, too many industry organizations, and a number of companies, working on the challenges of IP now. It will be most efficient for everyone and most effective in disseminating our results to transfer the work to other organizations.

What work in particular would you transfer?

A There are two primary programs. First is the QIP [quality-IP] Metric, which is up and running on its own Web site. It has been downloaded a lot and is widely used. The second program, which is not so mature at this point, is the IP-encryption effort.

So, what will happen to this work now?

A The VSIA board will continue to operate as a

steward for the work, overseeing the transfer of the projects to other organizations. This [stewardship] will include finding appropriate organizations to take up the projects, identifying corporate champions to continue driving the work, and seeding [the receiving organizations] with senior people from our working groups.

Then, you see the work going on, even after the organization formally has ended?

A Oh, absolutely. There is still a need for the work. But the IP industry has matured to the point that our members don't see a need for one more umbrella organization. Right now, we are at a point where all of our projects are stable enough to transfer, and it makes sense to continue them through other organizations.

Are you looking at any specific organizations to carry on the work?

A We have had discussions with people from the IEEE, and they have expressed interest in picking up the QIP effort. Other indus-



try organizations, such as the SPIRIT [Structure for Packaging, Integrating, and Reusing IP Within Tool Flows] Consortium and the Si2 [Silicon Integration Initiative], are also obvious possibilities.

It seems that there is strong interest in the QIP Metric in China, as well.

A Yes. There are senior people in China with some distinct ideas about QIP. Given the state of design practice in that country, they are interested in taking the QIP effort beyond being a metric for comparing IP offerings and making it into something like a cookbook for adopting and integrating IP into a new chip design. Some people there would like to see a government agency adopt QIP and administer IP reuse.

Are there areas of IP reuse in which you think more work is still needed?

A The whole IP-transfer process—the way specific information moves from

provider to user—is still being worked out. Today, it can involve a tangle of different file formats and deliverables, different for each IP vendor. Also, there's the area we call hardware-dependent software. We have not yet addressed the problem of evaluation and transfer of the low-level software that enables the semiconductor IP to function. But, as more and more IP becomes software-programmable, that software is becoming a key issue.

What do you think will happen to the people who have put so much work into VSIA programs once the transfer is complete?

A Well, many of them will go on working on the projects, because they are also members of the organizations to which we will transfer the efforts. As to the management, after the board formally stops meeting, I suspect we will still talk to each other about IP issues. It's a very small industry in that way.

—by Ron Wilson

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BY BONNIE BAKER



How the SNRs of delta-sigma converters differ

When I was a child, my parents bought me a 1-in.-diameter box turtle. I was so excited! To protect the turtle, I was going to put it in my block wagon. This wagon had slots to insert square, triangular, and round pegs. When my mom saw me grab a hammer, she knew it wouldn't be a pretty picture. "You can't fit a square peg—or a turtle—into a round hole," she told me.

That lesson also applies to the basic concept underlying delta-sigma modulators and ADCs—a concept that has been around since the 1930s. This converter topology is a bit different from other topologies; however, many engineers still strive to fit this converter into the standard ADC square hole.

Delta-sigma converters go beyond performing a simple analog-to-digital conversion. They have an oversampling mechanism, a modulator, and a digital filter. The oversampling mechanism spreads the noise power across a wider frequency range. The modulator shapes the low-frequency noise or pushes it out to higher frequencies. The digital filter averages the noise and eliminates it in the higher frequencies. The ideal successive-approximation-register and pipeline SNR (signal-to-noise ratio) is $6.02N+1.76$ (Reference 1), where N is the number of converter bits. The delta-sigma-converter SNR is $6.02(N+N_{INC})+1.76$, where N is the number of modulator bits and N_{INC} , the increase in resolution, is:

$$\frac{1}{6.02} \left[(20M+10)\log_{10} K - 20\log_{10} \left(\frac{\pi^M}{\sqrt{2M+1}} \right) \right]$$

In this formula, M is the order of the modulator, and K is the oversam-

Many engineers still strive to fit this [delta-sigma] converter into the standard ADC square hole.

pling ratio during the conversion.

Ideally, the delta-sigma-converter SNR, with a first order modulator, is $6.02N+1.76-5.17+30\log_{10}OSR$ where OSR is the oversampling rate and N is the number of modulator bits—not converter bits (Figure 1).

These ideal formulas assume that

the linearity, noise, and offset errors of the ADC and DAC—usually, 1-bit devices—are ideal and that the digital filter has an ideal brick-wall response. Actual delta-sigma converters are not as ideal as you would hope.

With these theories of the ideal, the best approach is still to rely on bench data for your converter performance. This data gives you a realistic view of the converter's capabilities. On the bench, you can measure your converter's rms noise by acquiring a few hundred samples of a dc-input signal. In this circumstance, the formula that describes any ADC SNR is $20\log_{10}(V_{RMS-FS}/V_{RMS-NOISE})$.^{EDN}

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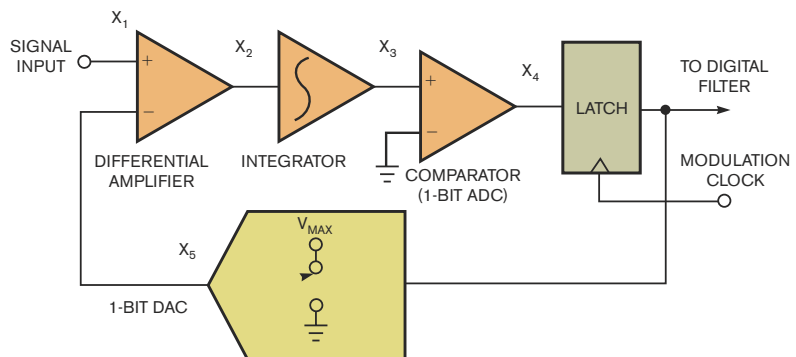


Figure 1 With a first-order modulator at the input of a delta-sigma converter, the ideal SNR is $6.02N+1.76-5.17+30\log_{10}OSR$.

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A digital picture frame is worth 1000 words



The explosive growth of digital cameras has created a problem: What do you do with all those photos? To deal with this problem, many camera owners are adopting a DPF (digital picture frame) to sequentially display a large number of images and as a replacement for the traditional photo album. *EDN* took a look at the inner workings of the Westinghouse DPF-0561. With a 5.6-in. LCD, 8 Mbytes of internal storage, and sockets for multiple plug-in memory formats, the DPF-0561 can display both JPEG still-image files and AVI (Audio/Video Interleave) full-motion files. The current price for the DPF-0561 is \$80 to \$120.

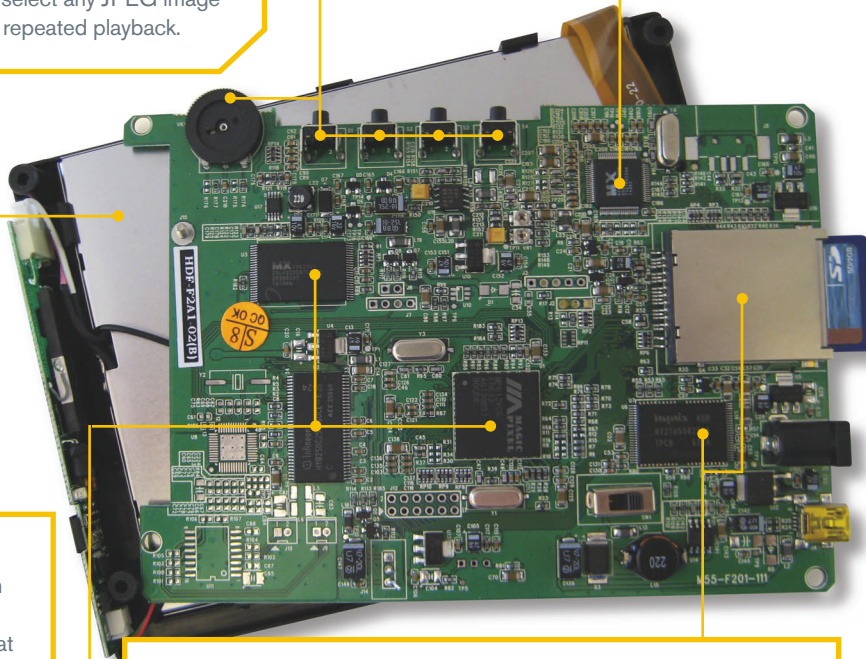
Unlike many of the simpler frame designs, the DPF-0561 includes several user controls with onscreen-display feedback. A rotary potentiometer controls display brightness, and a set of four push-buttons controls various functions depending on onscreen-menu modes. The user can select multiple transition effects, slide-show-display speed, memory location, photo orientation, and menu language. The menu options allow the user to select any JPEG image for continuous display or AVI motion file for repeated playback.

The device displays digital pictures and videos on a 5.6-in. AT056TN03 LCD from Innolux Display Corp. The display's size and 320×234-pixel resolution are barely adequate for a low-end DPF. Like most small LCD units, the display is transmissive; it illuminates pixels from behind with an LED backlight. Other display specifications include a 65° viewing angle, a 300-to-1 contrast ratio, 350-cd/m² brightness, and a 20-msec response time.

The heart of the DPF is the Magic Pixel MP612 multimedia playback controller with decoders for both JPEG and MPEG formats. The circuitry decodes JPEG images at 48M pixels/sec and 640×480-pixel MPEG-1/MPEG-4 video at 30 frames/sec. The MP612 includes extensive audio-processing features. For downloading data to internal memory, the MP612 includes a USB 2.0 interface controller. An Infineon HYB25D256 DDR 256-Mbit SDRAM delivers local processing storage for high-speed image decoding, and a 29LV320 flash memory provides processor program storage.

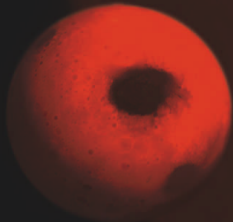
The MX88V44 TFT-LCD driver provides a single-chip drive for the 240×320-pixel-resolution quarter-VGA display. The driver accepts analog composite video in a 4:3 standard format as its input. Composite video, also known as CVBS (color, video, blanking, and sync), combines the brightness information (luma), the color information (chroma), and the synchronizing signals on one input pin. Portable televisions and DVD players widely use the MX88V44, supporting programmable brightness, contrast, and saturation.

The DPF-0561 boasts a range of picture-storage options. Users can download as much as 8 Mbytes of JPEG or AVI images directly over the USB connection to the internal Hynix Semiconductor NAND-flash memory. If you reduce the resolution to 640×480 pixels, the internal memory holds more than 80 images. The playback controller also includes interfaces for multiple external storage devices, such as smart media, memory sticks, multimedia, and xD-picture cards as well as micro drive and Ultra-DMA66 hard-disk drives. A CompactFlash connector is hidden on the back of the board.



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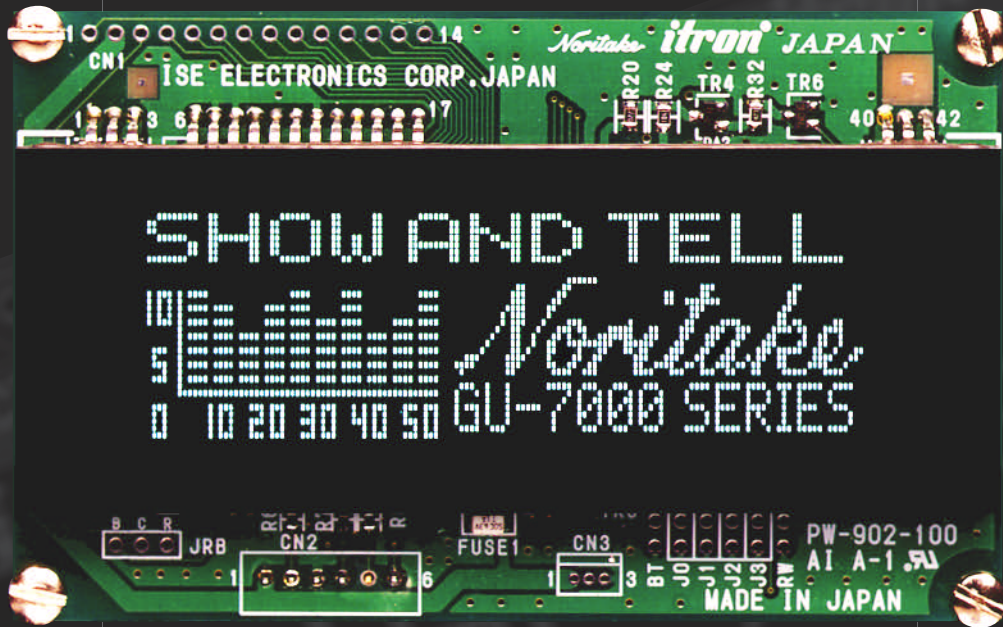
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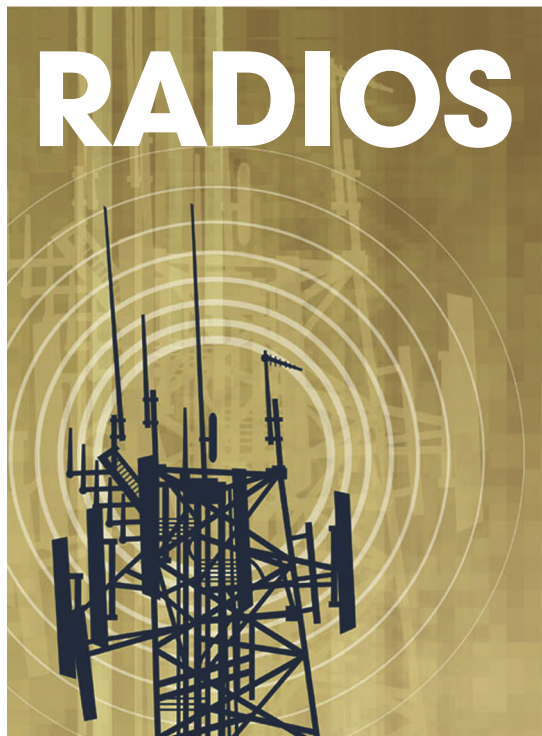
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RON WILSON • EXECUTIVE EDITOR



Wireless links are becoming ubiquitous in electronic systems. At high data rates demanding wireless connections, WiMax and 3G cellular dominate, whereas, at the other extreme, standards such as ZigBee and Wibree move data at far lower rates and energy-consumption levels. But, in all cases, market economics and consumer expectations demand that system architects at least consider integrating the radio hardware into an SOC (system on chip).

This demand raises some critical questions. First, is a single chip the best approach, or does isolating the radio on a separate die better serve the application? Second, given the answers to these questions, what are the best architectures to employ for the receiver and the transmitter? Underlying these questions are others: Can architects make these decisions in a systematic way, or must they make them not only case by case, but also with a case-by-case decision process?

Some vendors, particularly those in the cellular-handset market, seem to sug-

gest that anything less than a radio fully integrated into the SOC is as obsolete as the vacuum-tube tuner. Determining whether to implement a radio on a separate die using an RF process or to implement at least some of the RF circuitry onto the SOC in a vanilla-CMOS-logic process is far from obvious, however. The system architect must consider issues such as market expectations, life-cycle cost, performance requirements, and project risk. The architect reaches an informed decision only by assessing all these factors.

The first item on the list is an emo-

tional, rather than an objective, judgment. Particularly in consumer mobile markets, in which cost and form-factor issues are huge, a perception often exists that only a single-die approach is acceptable. "The pressure is to do a one-chip solution, even if [a one-chip design] is hard, and that means using digital CMOS," says Maryam Rofougaran, senior director of radio-technology engineering at Broadcom. "Even an RF-CMOS process tends to cost too much, so we target digital-CMOS processes."

Other vendors that play in the cellular-handset business, at least in segments with large volumes, agree. "For us, single-die is a business consideration only: We can make a business case only for a single-die solution," explains Robert Aiello, chief technology officer of Staccato Communications. "So, we have to build a team with experience in integrating radios for volume production."

Texas Instruments, perhaps the most insistent supporter of the approach, has gone so far as to brand its CMOS-single-die-radio architecture as the DRP (digital-RF processor). "There are clear benefits to a single-chip approach," says

Bill Krenik, TI's chief technology officer of the wireless-terminals-business unit. "Today, radio chips for low-cost applications are overwhelmingly done in digital processes," Krenik says. "But the design complexity and development cost are large for a single-chip architecture, so such a design requires a large market and good expected market share. A smaller segment, such as a high-end feature phone, might not make sense as a single-chip device."

Another view that you cannot ignore comes not from customers but from the venture-capital community. "I think that if you are a start-up today, your investors are going to push you to do a single-chip design in digital CMOS, whether you think that is the right approach or not," observes Teddy O'Connell, client manager at IBM. "But there are still very significant issues you need to look at before making the decision."

Many of these issues involve the cost of the approach. O'Connell and others point out that, as multichip packaging has become mainstream, the economics of single-die versus multichip designs have

AT A GLANCE

- ▣ Market forces are pushing integration of RF circuits into SOCs (systems on chips).
- ▣ There are still some compelling reasons to keep RF on a separate die.
- ▣ The choice of radio architectures—especially for receivers—is far from settled.
- ▣ The architect must think across the whole system, not just one chip.

changed. The budgetary cost of a two-die assembly may be greater than that of a single packaged die, but that difference is just the beginning of the equation. "That single die may be 20% RF circuitry, with significantly lower yield than the digital portion," O'Connell points out. "And, as the design migrates to finer geometries, the RF section may grow rather than scaling down. Further, the need for RF performance may push the entire design into a more advanced digital-process node than would have

been necessary if the design used separate RF and digital dice."

The cost question can be tricky, however. Choosing a single-die or multichip strategy can influence the choice of radio architecture, which in turn has significant influence over the number and quality of external passive components the radio will require. And those passives, after you pay for components, real estate, insertion, and test, can be significant factors in total system cost.

The questions of performance requirements and design risk also interrelate. On paper, it would appear that a 65-nm or even a 90-nm CMOS-logic process should work just fine for RF. "Just a few years ago, gigahertz-range RF meant GaAs [gallium-arsenide] processes with expensive transistors," observes Analog Devices' business-development director, Doug Grant. "But process shrinks have brought lower parasitic capacitances, shorter transit paths for carriers, and larger transistor budgets, all of which are benefits for RF designers."

Transistor cutoff frequencies in these processes can be greater than 40 GHz for

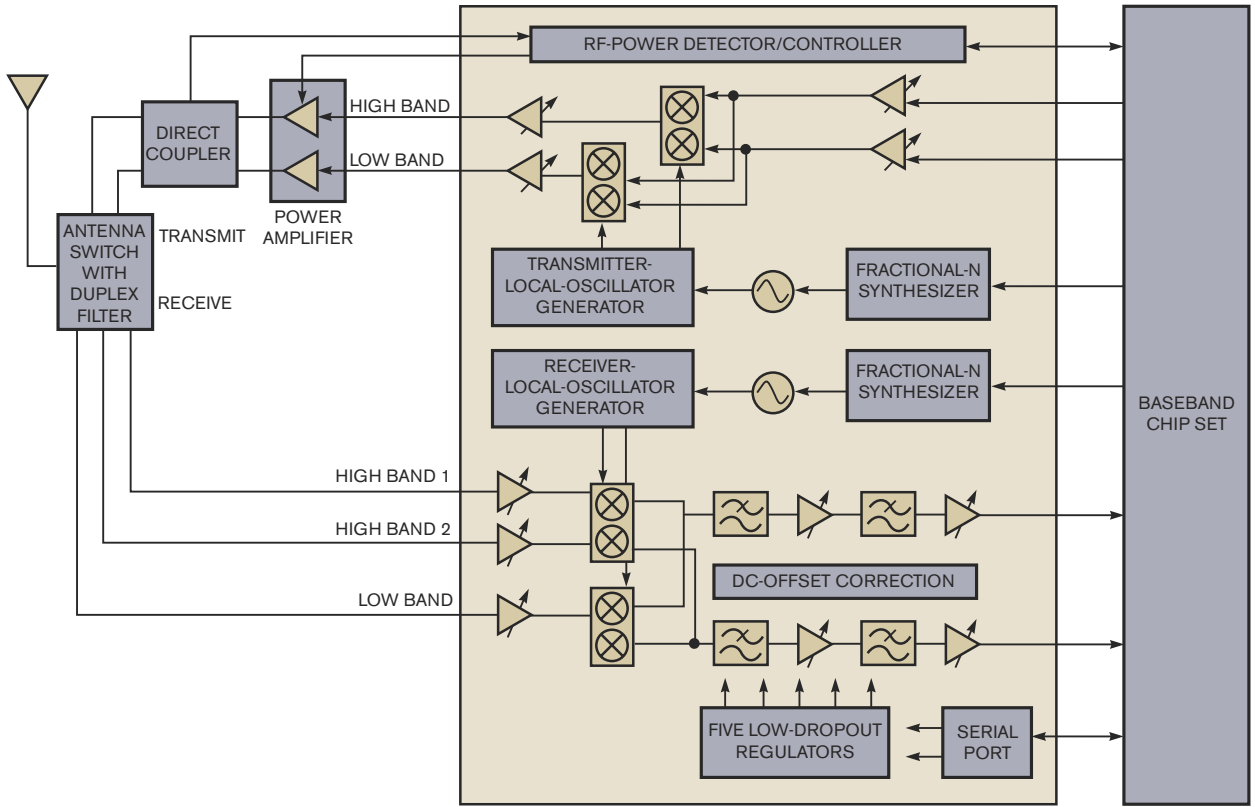


Figure 1 Analog Devices' single-chip radio for wideband-CDMA applications includes on-chip voltage regulators to stabilize delicate circuits.



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a 90-nm process and significantly higher for a 65-nm process. The lower series resistance of the small devices means that noise floors are lower, somewhat compensating for lower operating voltages. Linearity is not bad: “The third-order intercept is actually better in CMOS than it is in SiGe [silicon germanium],” says IBM’s O’Connell. And you can fabricate reasonably good spiral inductors, as long as the circuit does not require a very high Q.

So, why would anyone cite performance as a reason to use a specialized RF process on a separate die? There are plenty of reasons.

PROCESS AND PERFORMANCE

One good reason is frequency. “Regulatory requirements are pushing ultra-wideband radio links up to higher frequency bands. This [pressure] made operation at 10 GHz one of our design requirements,” says David Shoemaker, Alereon’s vice president of engineering and operations. “At that frequency, CMOS is definitely getting closer to viability; it can be fast enough. But, at those frequencies, it doesn’t take much variation to have a significant problem. For instance, it’s easy for VCOs [voltage-controlled oscillators] to become unstable, and there are issues with gain flatness.” After looking at these issues, Alereon chose to implement its RF front end in a SiGe process, with a promised migration path to CMOS. “We have the option to migrate the circuitry,” Shoemaker says, “but, right now, doing so wouldn’t buy us much in improved cost.”

Aside from gain, architects considering CMOS for RF have to think about linearity. The sensitivity of a radio to non-linearity depends on the application and modulation scheme. “Standards can have a big impact on whether you can implement a radio in a given technology,” says Staccato’s Aiello. “For instance, in our world, we use QPSK (quadrature-phase-shift keying), not 64-QAM (quadrature-amplitude modulation), and that substantially reduces the linearity requirements on the RF section.”

Another serious issue with digital CMOS is models. When high-frequency models are available at all for digital-CMOS devices, they are usually digital models. There is often little or nothing in the way of small-signal models.

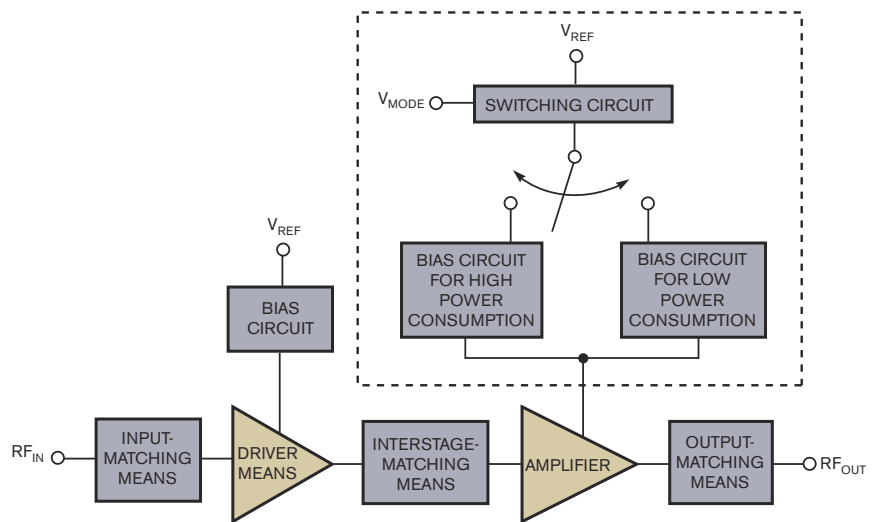


Figure 2 Even a simple RF amplifier must use a high level of digital intervention.

“Models are always an issue if you are an early RF user on a process, whether it’s CMOS or not,” says Dave Wright, lead systems architect at Cypress Semiconductor. “Even the BiCMOS process we use for our wireless-USB products was originally designed for high-speed-communications circuits, not RF. It was well-characterized but at different operating points than the ones we used.”

The transistor models are not the only issues. Noise models—especially good models of noise propagation through the power supplies and substrate—are essential. This situation is true for any RF design in which low operating voltages make noise an issue. It is also true in systems such as transceivers with on-chip power amplifiers and designs using multiple antennas in which multiple uncorrelated RF signals are present. Even if the models appear good, you’ll have the nagging worry that process engineers get paid to get good yields on big digital designs. They aren’t necessarily keeping careful watch over small-signal RF-model parameters while they cen-

ter their processes for gates and SRAM cells. This situation makes it almost incumbent upon a design team using digital CMOS to have its own modeling group and a strong enough relationship with its foundry to calibrate its own models.

When uncertainties with the models exist, the design has added risk, which is difficult to quantify. Despite that difficulty, designers must include that risk in their decisions. If a plausible risk of a design spin—or three—is unacceptable, they have two alternatives. One is to rely on a proven design team and a mature RF process. The other is to rely on digital calibration of the RF circuits to compensate for the uncertainties in models or variations. “Basically, we put compensation where we are least confident in our models,” says Analog Devices’ Grant. He says that it is not unusual for ADI designers to use 20 or 30 additional transistors in what would have been a simple bias generator, just to stabilize the CMOS-signal path over the operating-temperature range. To control voltage variations within the CMOS die, the company sometimes implements low-dropout regulators adjacent to delicate RF circuits (Figure 1). Alternatively, designers may employ digital techniques: using an ADC to make on-the-fly measurements of a circuit’s operating point, computing compensation parameters, and load-

(continued on pg 36)

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Comprehensive Fault Protection Features Designed for High-Reliability Systems Using LM3743 Controller

Application Note AN-1669

Ricardo Capetillo, Applications Engineer

Data center facilities and telecom basestation subsystems must manage the balance of two essential commodities—power and cooling capacity. For example, processors in rack-mounted servers demand large amounts of power and are one of the greatest sources of heat during normal operation. Substantial increases in heat during normal operation and fault conditions will reduce the reliability of many components in the server racks including semiconductor components, hard drives, and fans. The LM3743 controller will minimize power consumption during fault conditions thereby reducing thermal loads and increasing reliability.

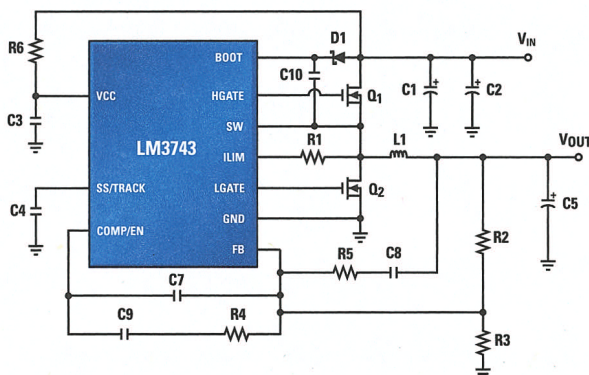


Figure 1. Typical Application Circuit

The LM3743 is a DC-DC voltage mode PWM buck controller featuring synchronous rectification at 300 kHz or 1 MHz. It can deliver current as high as 20A and step down from an input voltage between 3V and 5.5V down to a minimum output voltage of 0.8V. It is a highly integrated device in a small MSOP-10 package. Features include; pre-biased soft-start, tracking capability, and comprehensive fault protection features suitable for high-reliability systems such as rack mounted servers and telecom basestation subsystems.

LM3743 Comprehensive Fault Protection Features

The LM3743 provides the following comprehensive fault protection features: High Side Current Limit (HSCL), output Under-Voltage Protection (UVP), and Low Side Current Limit (LSCL). When engaged, these three features can each independently initiate a hiccup protection mode which disables both the high-side and

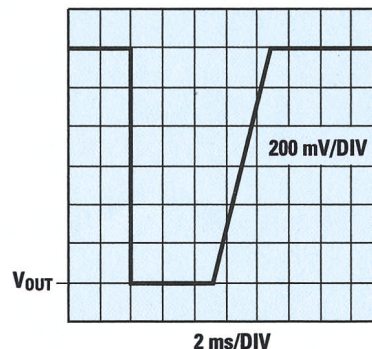


Figure 2. Hiccup Time Out and Internal Soft-Start

low-side FETs and begin a cool down period of 5.5 ms, see Figure 2. At the conclusion of this cool down period, the LM3743 performs an internal 3.6 ms soft-start to check for the removal of the fault condition and to continue normal operation. Hiccup protection mode enables the system designer to avoid the need to over design components due to thermal runaway during fault conditions resulting in a lower bill of material cost.

To help quantify the power consumption during a persistent fault condition, let us examine an application with a 10A low-side current limit. Once in overload, the low-side current limit controls the valley current and only allows an average of 10A plus the ripple current to pass through the inductor and MOSFETs. Hiccup mode initializes after 15 switching cycles allowing only a very small temperature rise. Once in hiccup mode, the average current through the high-side FET is:

$$I_{HSF-AVE} = (I_{CLIM} + \Delta I) \times [D(15 \text{ cycles} \times T_{SW})] / 5.5 \text{ ms} = 71 \text{ mA}$$

With an arbitrary $D = 60\%$, ripple current of 3A, and a 300 kHz switching frequency.

The average current through the low-side FET is:

$$I_{LSF-AVE} = (I_{CLIM} + \Delta I) \times [(1-D) \times (15 \text{ cycles} \times T_{SW})] / 5.5 \text{ ms} = 47 \text{ mA}$$

And the average current through the inductor is:

$$I_{L-AVE} = (I_{CLIM} + \Delta I) \times [(15 \text{ cycles} \times T_{SW})] / 5.5 \text{ ms} = 118 \text{ mA}$$

Protecting Typical Fault Conditions in High-Reliability Systems

Server racks and telecom basestation subsystems require high reliability to enable uninterrupted flow of data and communication. When unexpected failures occur, the LM3743 fault protection features can help to prevent further electrical and thermal stress. Examining some typical system fault conditions, we can elaborate on the protection modes of the LM3743 device and the operational benefit:

Example 1:

A capacitor such as a POS-cap located at the output of the LM3743 fails as a short circuit after an over-voltage surge exceeds the maximum capacitor voltage rating, refer to *Figure 3*. In such a situation, duty cycle and the inductor current increase cycle by cycle, but fortunately input current is decreased because the UVP of the LM3743 initializes hiccup-mode.

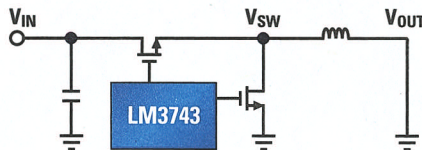


Figure 3. Output Short-Circuit to Ground

Example 2:

A small piece of metal falling into the product from the outside or a piece of metal that was loose in the product changes positions during shipment and lands across the switch node (V_{SW}) and ground, see *Figure 4*. High-side current limit immediately senses the short circuit fault condition.

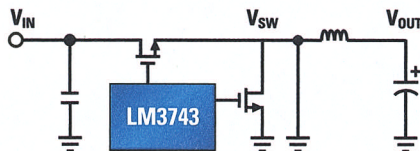


Figure 4. Switch Node Short-Circuit to Ground

Example 3:

Excessive load and/or incorrect selection of the MOSFET results in an open circuit failure. For example; if the low side MOSFET (Q2) fails, depicted in *Figure 5*, the inductor current will not flow during the time Q2 should be on, thus the inductor current will increase cycle by cycle. The high-side current limit will capture the over-current event, thereby protecting the high-side MOSFET (Q1) from over heating and failure.

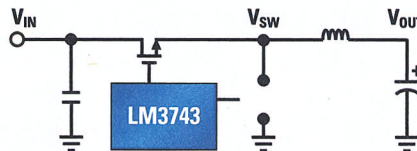


Figure 5. Low-Side MOSFET Open-Circuit Failure

In each example, the LM3743 provides fault protection, reduces the average input current, and relieves the power components from thermal stress during persistent fault conditions. After the removal of the fault condition, the LM3743 performs an automatic self test and recovery sequence. User intervention is not required, therefore reducing maintenance cost and designed in circuit complexity.

The LM3743 provides comprehensive fault protection and a reduction in server power consumption during fault conditions. It also combines high efficiency with high drive capabilities for loads up to 20A. With the LM3743, the balance between power and cooling capacity are much more manageable during device failure and short circuit conditions. ■

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(continued from pg 32)

ing a DAC to adjust a bias or offset (Figure 2). Some designers joke that they are moving to a design style that has the output of a DAC attached to every terminal on every RF transistor.

“There’s no question that making a radio scalable is a digitally intensive process,” says TI’s Krenik. “Linearity, for instance, is one of the fundamental challenges. Old-school design said you had to have a very-high-linearity, high-voltage front end. But, with today’s processes, you have to let go of that notion. Now, we use precise digital control over bias and a few other parameters to linearize a less-well-behaved circuit.”

But this level of control in itself introduces another issue into the single/die controversy. “Power is one of our most important parameters,” says Adam Gould, senior vice president of product development at NextWave Wireless. “Normally, you would assume that an older process would require more power. But, in CMOS, you spend power consumption to get linearity. In WiMax, for instance, achieving sufficient linearity in the power amplifier is one of the biggest issues in the power budget. Right now, an optimized RF process is giving us better power consumption.”

So, the question of one chip versus two is not clear-cut for everyone. In some markets, there is no practical choice: The market expects a single-die approach, and the cost ceiling demands it. In these markets, a typical implementation might be a baseband digital-CMOS SOC integrating a radio. In other markets, a multichip package may allow the design team to go either way, and the decision depends on performance and power requirements, the choice of radio architecture, the availability of stable models, and the experience of the team. “You see both digital CMOS and SiGe RF in wideband-CDMA today,” IBM’s O’Connell says. In yet other areas, particularly at 10-GHz and higher frequencies, no practical alternative

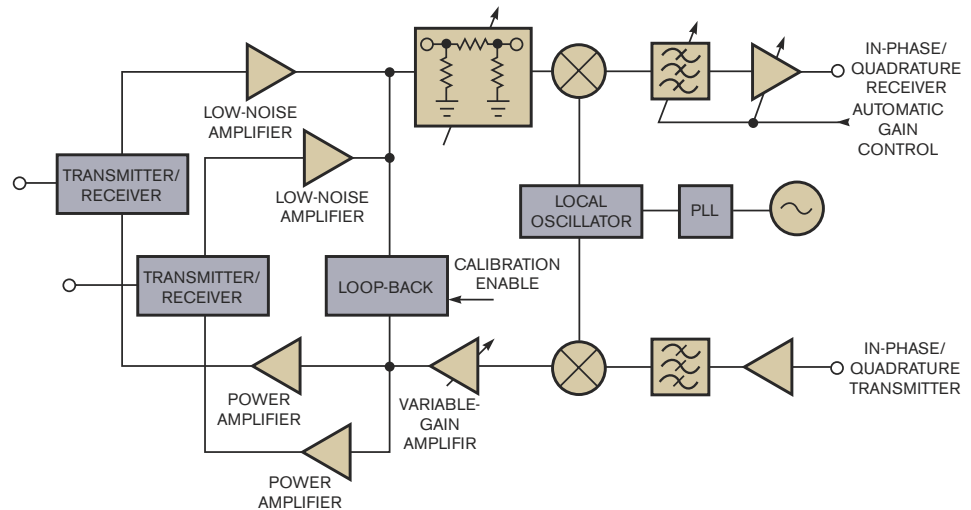


Figure 3 The 10-GHz Alereon ultrawideband-radio chip exemplifies the most common receiver architecture: the directly coupled receiver.

yet exists to RF processes for receivers. “WiMax, 5-GHz networks, and radars are still clearly SiGe applications today,” O’Connell says. Note, however, that the frequency at which a specialized process such as SiGe or GaAs becomes necessary can be considerably lower for power amplifiers and antenna switches, which involve significant power, than for receivers.

For power amplifiers, other issues arise beyond just the choice of process

ON THE RECEIVER SIDE, THERE IS A GROWING PREJUDICE THAT, THE SOONER YOU CAN DIGITIZE THE SIGNAL, THE BETTER.

technology. “As your effective channel length gets shorter, the problem of an integrated power amp gets harder and harder,” says Rofougaran. “The very small transistors can’t tolerate large signals for a number of reasons, including reliability and local heating. There can be really huge currents involved in power amps under some operating conditions.” Despite that fact, Rofougaran says, Broadcom does integrate the power amp in some low-power appli-

cations, such as some of the company’s Bluetooth chips.

“Technically, it’s feasible to integrate any power amplifier up to about 10 mW. But about 4 mW is the practical limit today,” says Cypress’ Wright. “Beyond that level, you have structures in the power amp that start consuming significant amounts of static power even in low-power modes, eating into battery life. Voltage swing can also be an issue, especially with more advanced processes.”

RADIO ARCHITECTURES

Decisions about one die or two interact with decisions about the radio architecture designers will implement. These decisions include choices for both the receiver and the transmitter sides of the radio. On the receiver side, there is a growing prejudice that, the sooner you can digitize the signal, the better. Some vendors have experimented with placing an ADC on the output of the low-noise amplifier and directly digitizing the incoming RF with only a band-pass filter between the converter input and the white-noise world. At the other extreme, some designers continue to use superheterodyne-receiver architectures that date back to the early days of vacuum-tube radio. As usual, the most frequently chosen architecture—the direct-conversion receiver—lies somewhere in between.

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HIGH PERFORMANCE ANALOG

In many ways, just putting an ADC on the low-noise amplifier—or, for that matter, the antenna—would be ideal. This approach largely eliminates the problems and pains of RF design and gives rise to new possibilities. For instance, a cellular base station that simply digitizes the entire cellular spectrum could simultaneously filter bands and select channels for many modulation schemes. Designers would then not need to assign an RF front end to each active session, and the quality of filtering in the digital domain could be superior to anything a physical filter could achieve.

“But the converter for such a design would be very difficult and, in any case, would take plenty of current,” says O’Connell. To capture enough information for the digital processing to succeed, the converter would have to have an enormous sample rate; a large dynamic range, so that the DSP could extract small incoming signals from powerful neighboring-channel signals and out-of-band noise; and, for similar reasons, superb linearity. Although such a converter design is now possible, O’Connell believes that it would currently be feasible only for high-end designs, such as base stations and multistandard “world phones.”

A better choice, in the view of most radio architects these days, is a direct-conversion receiver (Figure 3). In this architecture, the RF signal passes from the low-noise amplifier into a mixer stage that multiplies the RF signal by I (in-phase) and Q (quadrature) signals from a local oscillator. The resulting products are two signals—I and Q—already at baseband frequency. Normally, the baseband signal goes through an antialiasing filter into a pair of ADCs.

This approach doesn’t make things particularly easy. The direct-conversion architecture emerged in the early days of vacuum-tube radio soon after the superheterodyne, but designers abandoned it because of its challenges. The low-noise amp and mixer still must be linear. The local oscillator still must be clean and stable, and the suitability of the direct-conversion architecture depends to some extent on the modulation scheme. “It depends on the data,” says Broad-

com’s Rofougaran. “In our 2046 Bluetooth chip, we are dealing with GFSK (Gaussian-frequency-shift keying) that has a relatively narrow data bandwidth but puts a lot of the information spectrum close to dc. A direct-conversion architecture would be a problem, because of the issues with dc-offset cancellation. So, we use a low-IF superheterodyne arrangement. In contrast, wireless LANs have relatively wide data bandwidths and little information near dc, and we use direct-conversion architectures for them.”

Cypress also opted for a low-IF superheterodyne architecture for its wireless-USB device. “It was optimal for our situation,” Wright explains. “We have a good circuit design and are getting better spurious rejection than others using direct-conversion architectures. And, with the low IF, we are not burning a lot of power in logic circuits. We could have moved to direct conversion at some point, but it’s sometimes best to just reuse an existing architecture.”

One issue that works against the superheterodyne is the difficulty of system integration of a receiver employing the approach. Alereon’s Shoemaker points out that IF sections tend to generate frequency spurs that aren’t necessarily a problem for the superheterodyne receiver itself but can wreak havoc with other receivers in the system. Because many mobile devices these days contain multiple radios, system architects must carefully plan the frequency spectrum for all the radios in the package—before designing the devices.

Similar decisions arise on the transmitter side. Here, the most common architecture appears to be the polar-loop power amplifier. This design, incorporating feedback loops for both amplitude and phase signals, provides good linearity in both amplitude and phase—important for modulation schemes such as QAM that encode information using both quantities. However, designers have discussed other schemes, including futuristic ones, such as directly driving the antenna with a power DAC.

So, in decision-making for radios on SOCs, growing pressure from end markets and investors urges manufacturers to go to single-chip designs, at least

with small-signal RF circuitry. Designers using this approach must overcome formidable problems in integration, however. Many of these problems respond to the aggressive use of digital circuitry for calibration and control and to design experience. But the industry is a long way from the day when high-frequency receiver-RF stages will as a matter of course go onto SOCs and even further from the day in which any but the lowest power transmitter circuits will dwell there.

Because CMOS-process technology is not moving in the direction of greater friendliness to RF design, increasing integration will likely mean—as it did several years ago at TI—significant innovation in circuit design and in radio architecture. Analog Devices’ Grant makes an important observation about how designers achieve progress in this direction. “On a project a few years ago, we stood back and looked at the whole design,” he says. “We realized that the RF, digital, and software designers really didn’t talk to each other much. They were all working on their own separate noise budgets, and that [situation] was leading to some real inefficiencies in the system. We realized at that point that you have to optimize across the whole signal chain. You can’t separate the blocks from each other. And you have to look at the whole radio, including the filters, the digital controls, and the operating modes the software creates; you can’t just look at the silicon.” **EDN**

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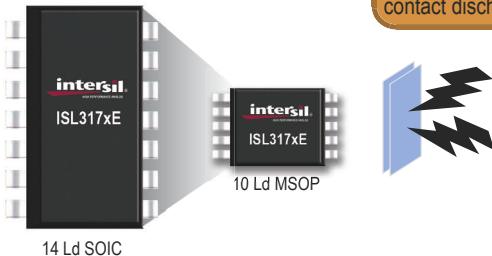
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ISL3172E	0.25	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3173E	0.5	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3174E	0.5	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3175E	0.5	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3176E	20	No	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3177E	20	No	No	8 Ld MSOP, 8 Ld SOIC
ISL3178E	20	No	Yes	8 Ld MSOP, 8 Ld SOIC

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HOME TRANSPORTATION:

Most home LANs (local-area networks) today serve simply to share a broadband link or printer; however, the situation is rapidly transforming. Broadband access is evolving beyond its e-mail, text-messaging, and Web-surfing roots into areas such as VOIP (voice over Internet Protocol), videoconferencing, multimedia streaming, and music and video rentals and purchases; today's early-adopter power users are driving these applications. And, once that multimedia content enters the premises, consumers aspire to spread it throughout the home in an interclient fashion (**Reference 1**). These trends have three fundamental impacts on the home LAN: First, the LAN "footprint" must pervasively extend across the

premises. Second, the LAN must deliver sufficient performance to allow multiple clients to simultaneously access it in a bandwidth-intensive fashion without perceived degradation in quality. Third, LAN latency also becomes a critical parameter; delay-sensitive interactive applications, such as Internet telephony, videoconferencing, and online gaming drive the need for low latency.

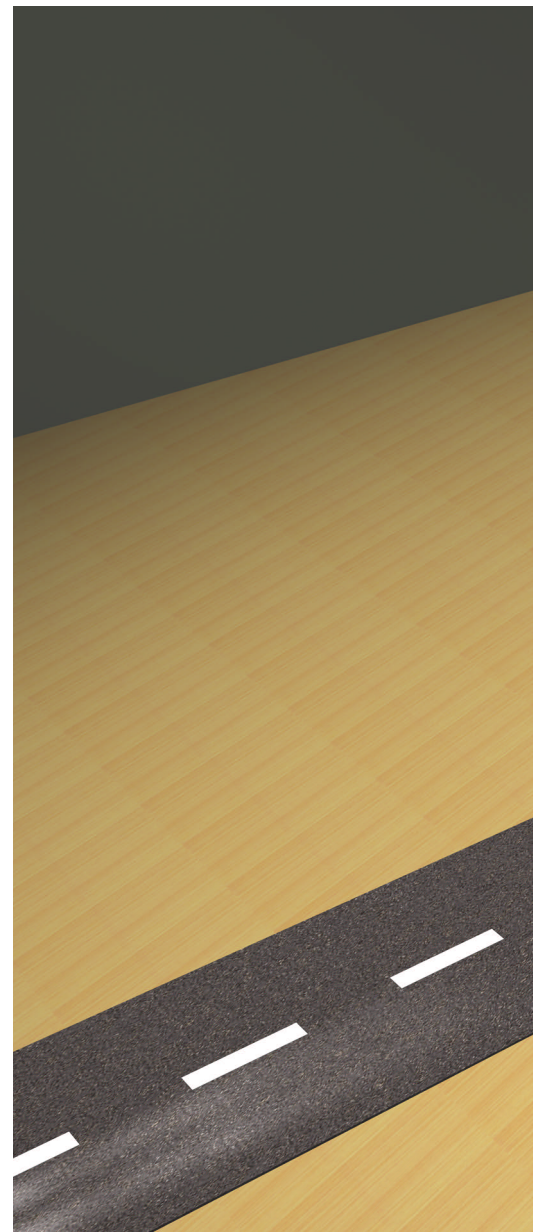
The tipping point at which the network-performance expectations of a critical mass of consumers will rapidly and dramatically increase is looming on the horizon, and it's often advancing on multiple parallel fronts. From a latency standpoint, for example, look at the booming popularity of VOIP services, such as Skype, and of gaming services, such as Microsoft's Xbox Live and Games for Windows Live and Sony's PlayStation Network. And, speaking of gaming, all three of today's leading consoles—Microsoft's Xbox 360; Sony's PS3; and Nintendo's Wii, which

works in conjunction with third-party software—can act as media extenders, decoding and playing content that's housed on and streamed from a computer, NAS (network-attached-storage) box, or some other LAN client (**Reference 2**).

The emerging multimedia LAN migration served as the root motivation for this hands-on project. This report evaluates various networking-technology alternatives, with the goal of assembling a cost-effective, simple to assemble, easy-to-operate, robust, and high-performance network.

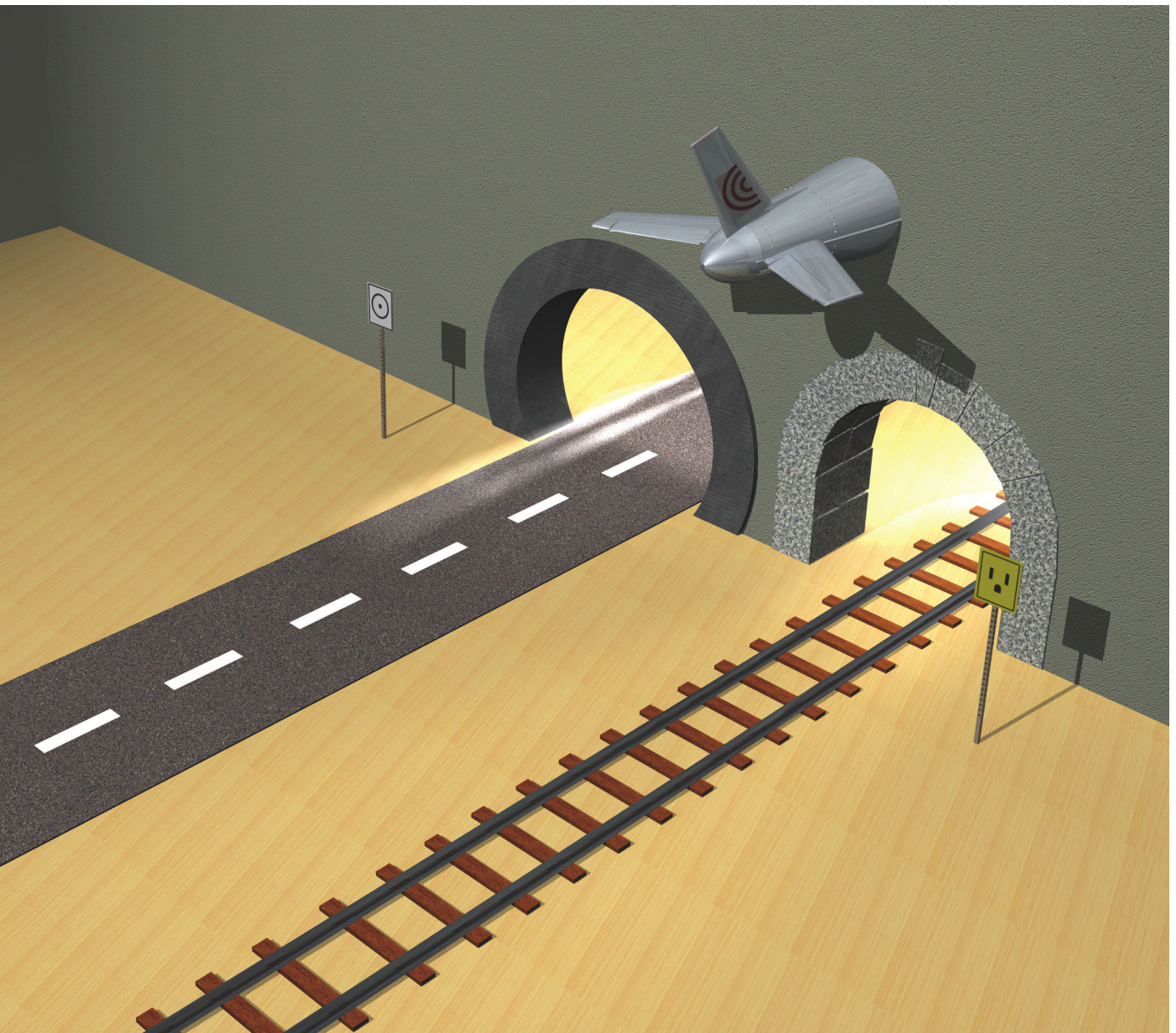
ASPIRATIONS AND BOUNDARIES

Benchmarking projects such as this one are fraught with potential peril. As I noted in an earlier article, up-front assumptions can heavily influence outcomes (**Reference 3**). "If I select a combination of equipment, software, and usage-model variables that are too specific, my results would be meaningful to



HOME NETWORKS CARRYING HIGH-DEFINITION VIDEO AND OTHER LARGE-DATA PAYLOADS NEED AMPLE BANDWIDTH AND CONSISTENT PERFORMANCE. CAN POWER-LINE TECHNOLOGY FIT THE BILL FOR LONG DISTANCES, OR MUST CONSUMERS RESIGN THEMSELVES TO STRINGING CATEGORY 5 CABLE? AND WHICH 802.11 STANDARD WILL SUFFICE FOR SHORTER DISTANCES?

BENCHMARKING POWER LINE, 802.11, AND ETHERNET



only a narrow set of readers,” I wrote. “Choose a too-broad set of options, on the other hand, and I end up with a bewildering plethora of outcome data.” These statements apply equally well to this report.

The intrinsic performance capabilities of two pieces of equipment can significantly influence the robustness of the network connection between those two pieces of equipment. With a traditional Category 5e-cabling topology, the routing and switching gear that establishes and maintains the connection is an additional notable factor, as is any other equipment on the LAN that might also be contending for network access. And with power-line and wireless networking, the list of potential influencers further broadens. In the case of power-line networking, sources of impressed noise can affect the fundamental robustness of the power grid, and, in the case of wireless networking, transmitter-to-receiver distance, intermediary walls, and other environmental attenuators, along with other wireless devices that inhabit the same portion of broadcast spectrum, can degrade signals.

Although some optimistic 802.11 and UWB (ultrawideband) backers might claim that wireless can be the *only* networking technology necessary to connect the home, reality often intrudes on this Pollyanna prognosis with pragmatic results. In my case, for example, my approximately 2000-square-foot, single-story property requires *four* conventional 802.11g access points to ensure a suf-

AT A GLANCE

▣ This article assumes that 802.11 has sufficient range to span one to several rooms but not an entire household, thereby requiring a companion backbone technology, such as Category 5e cabling or power line.

▣ Equipment and environment specifics can potentially shackle an otherwise-speedy networking technology; you must understand up-front assumptions to accurately assess benchmark results.

▣ Newer approaches' targeting of the UDP (User Datagram Protocol) is evident from my Iperf-generated statistics.

▣ Power-line networking has made tangible generational improvements in speed, reach, and inherent reliability.

▣ This article exposes why 802.11n's "draft" moniker is still justified, but the technology exhibits tremendous promise.

ficiently pervasive coverage footprint (Reference 4). I suspect that Faraday-cage-creating chicken wire in my walls, a common construction technique of multiple eras and regions, is one key culprit. Granted, the MIMO (multiple-input-multiple-output) antenna configurations in 802.11g-derivative and draft 802.11n equipment reportedly notably stretch a wireless network's reach. But I resisted the urge to do long-distance 802.11 benchmarking, in no small part

because I was concerned that the results from such testing from my home-office setting wouldn't broadly apply to other operating environments.

In reaching this decision, I also kept in mind the ever-increasing ISM (industrial/scientific/medical) broadcast-spectrum corruption; nearby neighbors' 802.11 networks and other wireless-broadcast sources, such as microwave ovens, cordless phones, and Bluetooth-inclusive equipment are the causes of this corruption. And a wireless-only network approach is of no direct benefit to LAN gear that doesn't embed a wireless transceiver; an external wireless bridge is a cumbersome and expensive "Band-Aid" in such a case. Instead, referencing the home topology in Reference 4, my wireless testing involved line-of-sight connectivity spanning approximately 10 feet between a laptop in the southwest quadrant of my office and an access point in the room's northeast corner (Figure 1). For the LAN backbone, I compared and contrasted two wire-based approaches: traditional Category 5e cabling in both 100-Mbps and 1-Gbps Ethernet flavors and five variants of power-line-networking technology. The power-line spurs terminated in the swamp-cooler closet and our backyard hut; past analysis has identified both locations as being challenging power-line nodes (Reference 5).

The Web-exclusive sidebar, "Multimedia-home-LAN test bed," at the Web version of this article at www.edn.com/070802cs, details the topologies and

WEB-SITE SUPPLEMENTS WRAP UP THE WRITE-UP

Another day, another article too big to fit into the available print pages. Fortunately, there's room on the EDN Web site for the rest of the story. You will find supplementary material for this article both at its online version at www.edn.com/070802cs and at the Brians Brain blog at www.edn.com/briansbrain.

The Web version of this article expands on this print version with the sidebar "Multimedia-home-LAN

test bed, which contains information on equipment and environmental factors, along with additional graphics and two extensive data tables.

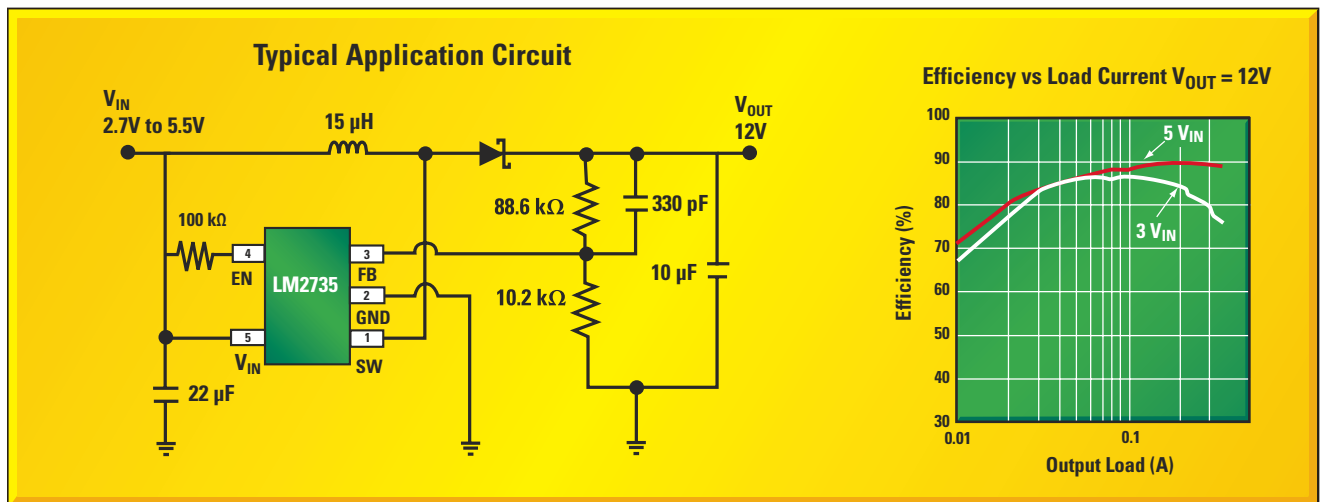
At Brian's Brain, "The missing-persons report" explains why I omitted other networking approaches in this study. "Next-step opportunities" suggests additional measures that you could take to advance the analysis I began with this project. "Results down-

loads and an additional-reading list" allows you to peruse my report files and screenshots to comprehend my logged data in greater detail, as well as suggests technical references to further cultivate your knowledge. "Share your thoughts," as its name implies, provides a forum for you to comment on data from this article that you find interesting, as well as to peruse and discuss the observations of your peers.

"Test-bed alternatives" recommends other network-performance-testing techniques, if Iperf doesn't work for you. And "Truth in marketing" provides more thoughts on the disparity between promoted and real-life-achievable network performance, including one egregious example. Visit the "Home transportation" post series at the Brian's Brain blog for these and other relevant networking postings.

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equipment used in my testing. I relied on the Iperf tool, which aims to measure network performance, as my project's benchmarking foundation. You can find more information on Iperf at <http://dast.nlanr.net/Projects/Iperf/>. Note, however, that, with Iperf, the *client* is the originating point for the TCP (Transmission Control Protocol) and UDP (User Datagram Protocol) data streams. The Iperf server, conversely, captures and logs the data coming from the client.

All the speeds for the power-line and wireless technologies I describe in this section refer to the peak PHY (physical-layer) rates, which differ from the real-life results that follow. My power-line-network testing began with Netgear's XE102 power-line-to-Ethernet adapters, which Netgear based on Intellon's HomePlug 1.0 14-Mbps transceivers (Figure 2). The XE102s came without a configuration utility, and none were available for download from Netgear's Web site. To examine the XE102s, however, I was able to use software from Belkin's site for the HomePlug 1.0-based F5D4070 as well as the Cogency Connection Manager, an older program from some Maverick Power Systems adapters that I owned. Stepping up performance a notch, at least on paper, is Aztech Systems' 85-Mbps HL105E power-line adapter, which the company also based on Intellon silicon, but, this time, of the proprietary HomePlug 1.0 Turbo variety. The Intellon-supplied PowerPacket utility enabled me to assess the adapters' reported bandwidth capabilities and other characteristics. I had previously upgraded the HomePlug 1.0 Turbo adapters to a firmware version that resolved UPNP (Universal Plug and Play) and other issues I'd initially encountered with them (Reference 6).

Further ratcheting up specified performance to the 200-Mbps threshold, three incompatible technologies vie for consumers' wallet contents. Linksys' PLE200 adapters employ Intellon's HomePlug AV transceivers, whereas Netgear's HDX101 power-line-to-Ethernet products implement DS2-designed technology, and Panasonic's BL-PA100 adapters use the company's internally developed HD-PLC power-line ICs. The three contenders' products all embed 100-Mbit Ethernet transceivers. Feel free to draw your own conclusions

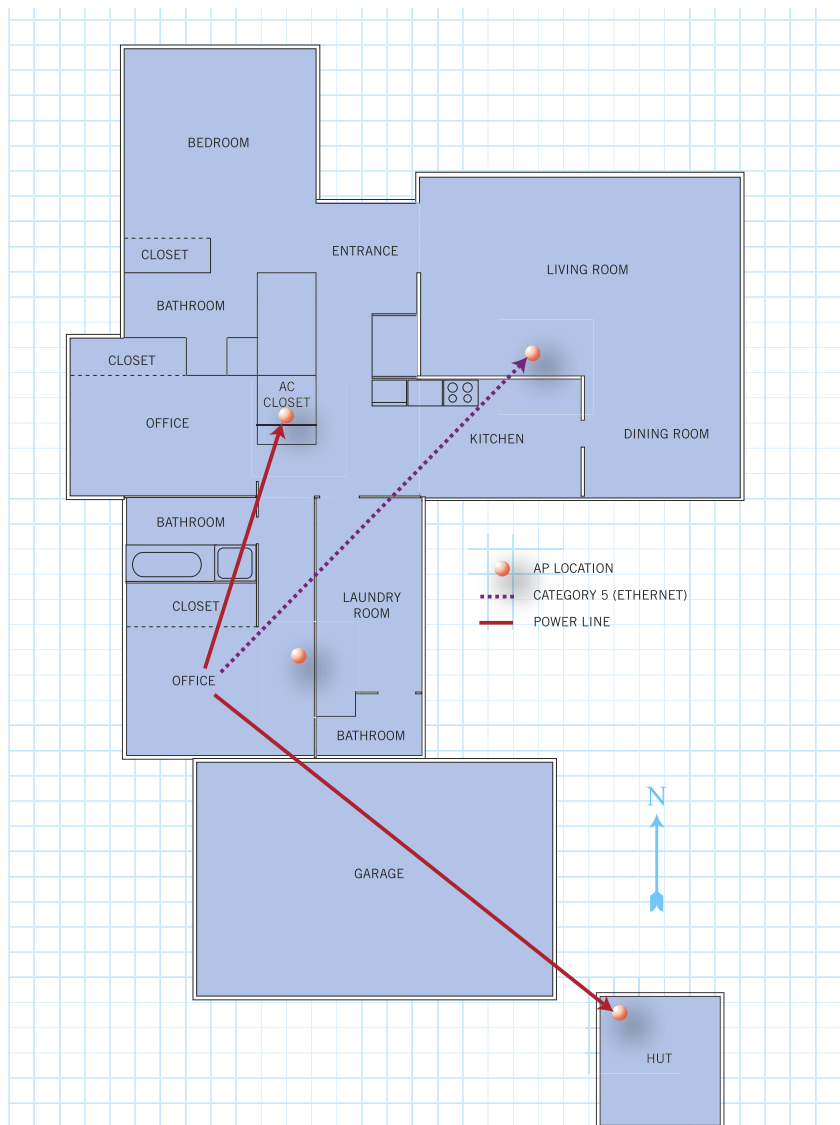


Figure 1 For this project, focus your attention on my office in the southwest corner of the house and on the power-line-network spurs running from it to the swamp-cooler closet and to the backyard hut.

about the disparity between marketing claims and real-life performance capabilities. Users can configure the DS2-based adapters for TCP, UDP, or no protocol prioritization; I ran tests on them in all three modes. Both the DS2- and HomePlug AV-based products also offer substantial per-service QoS (quality-of-service)-customization capabilities, which I didn't evaluate. The HD-PLC adapters are not user-configurable, but, based on the product specifications, I believe that Panasonic has optimized them for UDP traffic.

With all five power-line alternatives and in response to difficulties encountered with past power-line-networking

projects, I first paired the adapters with each other from adjacent power outlets within the same room before moving them to their under-test remote locations in the office, swamp-cooler closet, and hut. The power-line adapters' front-panel LED indicators reported and later testing confirmed that the existing pairings survived the relocations in all cases. In fact, the DS2-based Netgear-adapter pairings resurrected in the remote locations after I upgraded each adapter's firmware. However, somewhat irritatingly, to successfully execute the firmware upgrade, I first needed to temporarily relocate each HDX101 to a location with a direct Category 5 tether to the switch.

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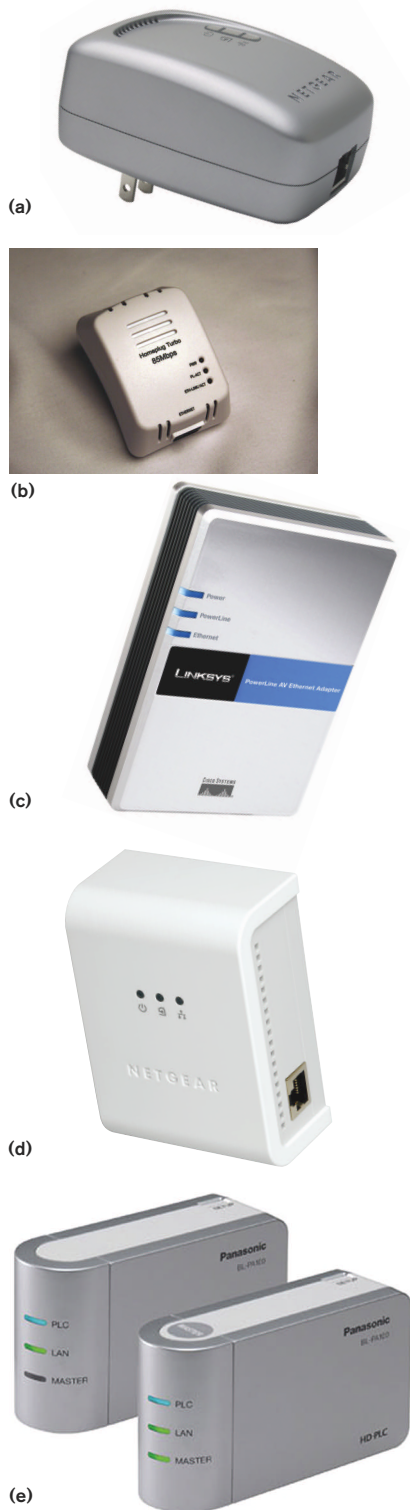


Figure 2 Power-line adapters include Netgear's 14-Mbps XE102 (a), Aztech Systems' 85-Mbps HL105E (b), and a triumvirate of 200-Mbps challengers: Linksys' HomePlug AV-based PLE200 (c), Netgear's DS2-based HDX101 (d), and Panasonic's BL-PA100 (e).

FOR SOME UNKNOWN REASON, IPERF DIDN'T RELIABLY GENERATE SERVER-SIDE GRAPHICAL REPORTS FOR UDP TEST RUNS.

The DS2-based adapters, which I had obtained in November 2006, were the only ones for which a firmware upgrade was available. I confirmed with DS2 that this upgrade version enabled the notch filters that protect ham-radio-broadcast-frequency bands from corruption and those that suppress interference with 27-MHz wireless keyboards and mice. Linksys' HomePlug adapters provided notch-filter protection only for the ham-radio bands, and, by press time, I could get no response from Panasonic on the presence or absence of any notch filtering in its HD-PLC adapters. I mention this fact not only because of any potential incompatibility issues with RF devices that might result, but also because active notch filters, which restrict power-line adapters' usable spectrum, tend also to reduce power-line adapters' effective performance.

To initiate my wireless testing, I pulled a Belkin F5D6130 11-Mbps 802.11b access point, from an earlier LAN incarnation, out of my garage inventory (Figure 3). Although a bit dusty, it still worked fine. For 54-Mbps 802.11g, I relied on the Belkin F5D7130 access point that currently populates my wireless LAN, and, for 54-Mbps 802.11a, I powered up an Intel Pro/Wireless 5000 access point that I'd previously purchased for \$4 from Surplus Computers (Reference 7). (The part's original manufacturer's suggested retail price was \$450.) I uncovered one minor issue with the Pro/Wireless 5000: I had to configure Iperf to limit UDP transfers to 50 Mbps or less; otherwise, the access point would lock up, requiring a power cycle to restore normal operation. Similarly, I had to hold UDP transfers through the Belkin F5D6130 wireless access point and the Netgear XE102 HomePlug 1.0 power-line adapter at or below 10 Mbps, but the speed limitation makes more sense in these cases because these products include only 10-Mbps Ethernet transceivers.

Most currently available 248-Mbps draft 802.11n access points and routers employ only the specification's 2.4-

GHz frequency band (references 8 and 9). At least two notable, dual-band—2.4- and 5.8-GHz—exceptions exist, however: Apple's Airport Extreme N router, which uses an Atheros Communications chip set, and Buffalo Technology's Wireless-N Nfiniti dual-band gigabit router and access point, which the company built on a Marvell Semiconductor silicon foundation. One key difference between the two products is that, whereas Apple's router includes a three-port, 100-Mbit Category 5 switch and similarly offers a 100-Mbit WAN (wide-area-network) port, the four LAN and one WAN connections on the Buffalo router are all GbE (gigabit-Ethernet)-capable. To test whether this disparity in performance potential would translate to a real-life differential, I disconnected the desktop PC from my LAN and instead connected it to the Apple and Buffalo products' LAN ports, thereby using them as routers versus employing them only as access points, as you can alternatively configure them. One other reason to nitpick about the Apple router was that, instead of providing a Web-browser-based configuration like the other access points and router I tested, it, like the power-line adapters, required that the user install a stand-alone OS X- and Windows-compatible administrator utility. I prefer the browser-based approach because the interface would be largely unaffected by obsolescence or changes in both operating systems and browsers.

THE RESULTS

My TCP and UDP tests ran for slightly longer than 10 seconds, and ASCII data-logged bandwidth measurements every second, both at the client and the server. I also captured post-test JPEG screenshots both at the client and the server for TCP test runs and at the client for UDP test runs. For some unknown reason, Iperf didn't reliably generate server-side graphical reports for UDP test runs. All of these files are available



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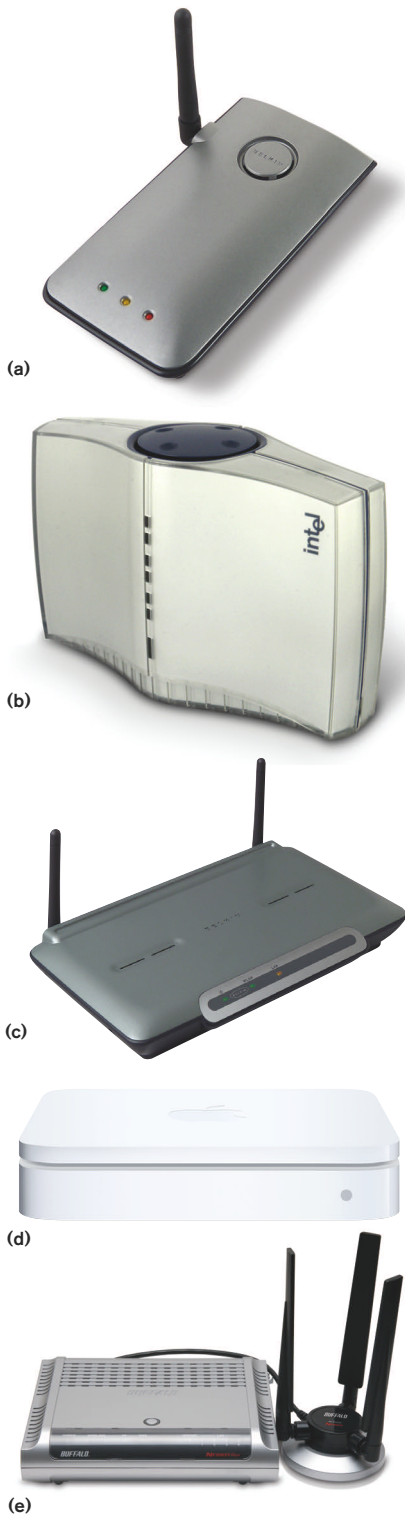


Figure 3 I tested four 802.11 wireless flavors, using five hardware platforms: Belkin's 802.11b-based F5D6130 (a), Intel's 802.11a-supporting Pro/Wireless 5000 (b), Belkin's 802.11g-implementing F5D7130 (c), and two draft 802.11n alternatives: Apple's Airport Extreme N router and access point (d) and Buffalo Technology's Wireless-N Nfiniti dual-band gigabit router and access point (e).

for you to download at the Brian's Brain blog (www.edn.com/briansbrain). (See also the sidebar "Web-site supplements wrap up the write-up.")

In sorting through the voluminous amount of data in Table A at the Web version of this article at www.edn.com/070802cs, you should first focus your attention on the TCP and UDP bandwidth reported at the server. As mentioned, the client generates the data streams, which I included in the table for completeness, and the server receives them; therefore, the server-side data provides the true measure of the intercomputer-communication channel's Category 5, power-line, and wireless capabilities. My impressions of the bandwidth statistics follow. I also welcome your observations and interpretations.

The sometimes-substantial bandwidth differential for data flow in one direction versus another surprised me. One notable example is the 48.5-Mbps average bandwidth for TCP transfers from the MacBook to the PowerEdge 400SC through the 100-Mbps switch, compared with a 0.33-Mbps average bandwidth in the opposite direction over the same connection. GbE TCP transfers showed similar degradation in the 400SC-to-MacBook TCP-transfer route. Although I operated each computer as both a client and a server, I didn't swap the computers' locations, so it's difficult to determine how much of this disparity was from the computers themselves and how much was from intermediary equipment or other aspects of the link between them. Nonetheless, I replaced the 16-port 10/100 Netgear switch with an eight-port 10/100/1000 switch from SMC Networks upon completion of my testing.

The significant disparity between TCP and UDP bandwidth and the comparative inconsistency of TCP bandwidth were also memorable. These results struck me even though I knew from my conceptual understanding of the two protocols' functions—that is, the source-to-destination "handshake" and, if necessary, packet retransmission in the case of TCP versus the absence of both these factors in UDP—that differences would exist (Figure 4). I can now understand why the power-line-networking promoters had been discouraged when, in my earlier online and print write-ups, I'd

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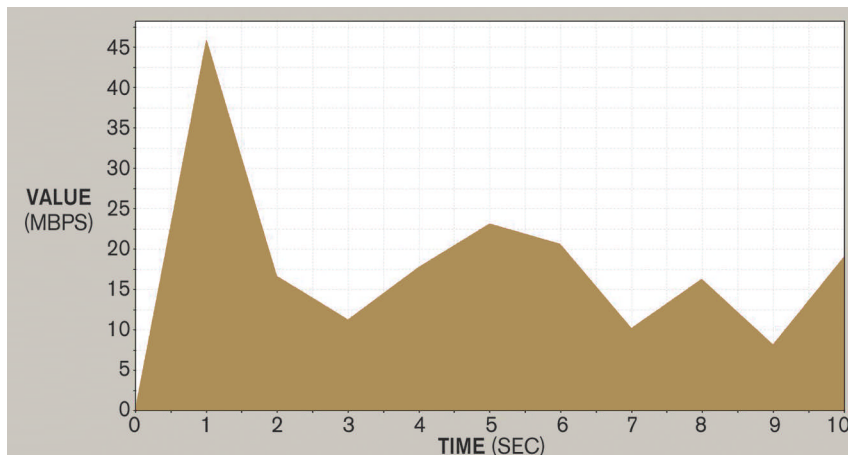
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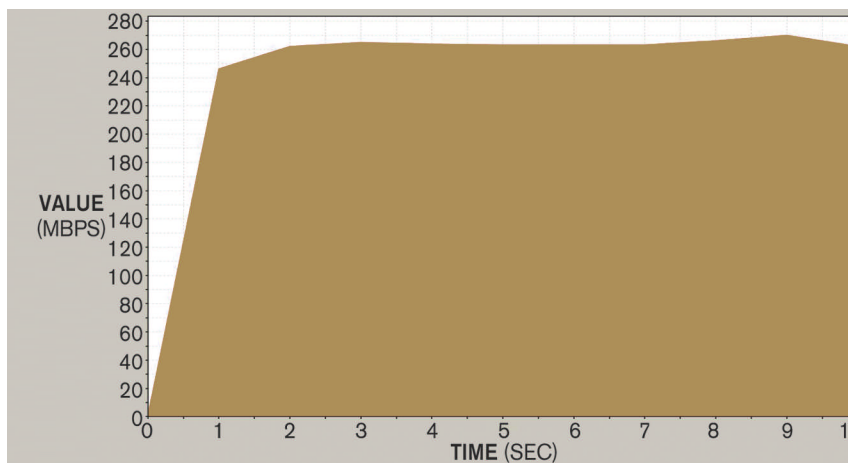
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(a)



(b)

Figure 4 TCP transfers (a) tended to be both more erratic and lower performance than their UDP counterparts (b).

focused only on TCP-based activities, such as file transfers.

On that note, I was impressed with the generation-to-generation UDP improvements that paced the HomePlug 1.0-to-1.0 Turbo-to-AV-technology transitions (Reference 10). Second- and later-generation power-line approaches have also made tangible improvements in overall robustness; whereas I had great difficulty maintaining a stable connection between the laptop and the desktop PC through the HomePlug 1.0 adapters, a situation I remembered well from past experiments, the other, newer technologies exhibited no irregularity in this regard. None of the 200-Mbps technologies delivered strong results for TCP transfers; the DS2 adapters were the leaders with this protocol.

Conversely, HomePlug AV was the

clear power-line winner with UDP, at least in my setup, and by a substantial margin. Look, too, at the three DS2 configuration options: TCP-optimized, UDP-optimized, and no protocol optimization; I'd be curious to hear your thoughts on whether you discern a clear and consistent correlation between the results you expect from the selected configuration option and those I obtained. In comparing the power-line data with that of the wireless alternatives, remember that the power-line spurs were dozens of feet long and encompassed a circuit-breaker-box intermediary, whereas the wireless connections were approximately 10 feet long and within line of sight.

For 802.11n, I was attempting to mate a Broadcom-designed wireless module in my MacBook with routers based on

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Atheros and Marvell ICs. The predictable immaturity of the draft 802.11n standard is, I think, evident in the results. TCP transfers through the Apple router were faster than those through the Buffalo router, due in part, perhaps, to the fact that the same company makes both the laptop and the former router and, therefore, they have more robust interoperability. However, for UDP transfers, the Buffalo router was notably superior in the achievable bandwidth it supported. The 2.4- and 5.8-GHz results for each router were largely comparable, at least in my 802.11-friendly configuration and environment.

In an alternative situation with polluted 2.4-GHz spectrum, on the other hand, the 5.8-GHz band might deliver demonstrably higher performance—at least at short distances. With all other factors being equal, 5.8-GHz signal strength degrades with distance more rapidly than does the 2.4-GHz signal strength. One other measure of draft 802.11n immaturity is that, after I switched the Apple router to 5.8-GHz mode, Windows' Wireless Network Connection Manager insisted that the laptop was no longer connected to the router, even though Apple's configuration utility and Windows itself in all other respects could still access it. **EDN**

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BRIEF

Conversion Latency in $\Delta\Sigma$ Converters

By **Bonnie C. Baker**
Senior Applications Engineer

Small-signal sensors often generate slow-moving DC signals. For these types of sensors, the $\Delta\Sigma$ ADC eliminates most of the analog input circuitry by providing a complete high-resolution, low-noise solution. Some systems have multiple sensors that may require a high-resolution, low-noise ADC with a multiplexer at its input. An example of a multiplexed sensor system is an automotive diagnostic application where numerous small-signal sensors monitor temperature, tire pressure, air-bag readiness, etc. (see Figure 1). Even though the sensors at the input of the multiplexer in these systems present low-frequency (nearly DC) signals, switching from channel to channel creates the need for an ADC that is capable of a high-speed response.

There are two common units of measure that describe the latency of an ADC: cycles and seconds. Cycle latency is the number of complete data cycles between the conversion initiation and the availability of the corresponding output data. Zero latency or 0-cycle latency is sometimes called no latency. Latency time, measured in seconds, tells the user how fast fully-settled conversions can be performed.

In the system in Figure 1, the multiple-channel ADC must have high resolution, low noise, zero-cycle latency, and low latency time.

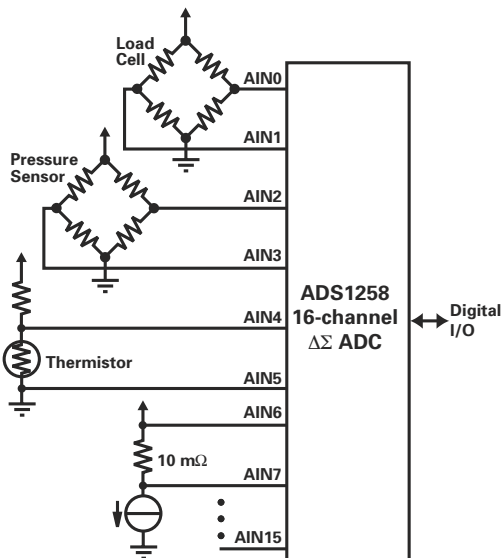
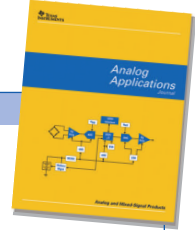


Figure 1: Example Multiplexed Sensor System

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ADC Cycle Latency

For ADCs, cycle latency is the number of complete data cycles between the initiation of the input-signal conversion and the availability of the corresponding output data (see Figure 2). The unit of measure for this definition of latency is N-cycle latency, where N is a whole number. Figure 2 shows the timing diagrams for a 0-cycle-latency (or zero-latency) ADC and a 4-cycle-latency ADC. In Figure 2(a), with 0-cycle latency, the sampling period of N+0 is initiated. The output data of N+0 is acquired before the sampling period of N+1 is initiated.

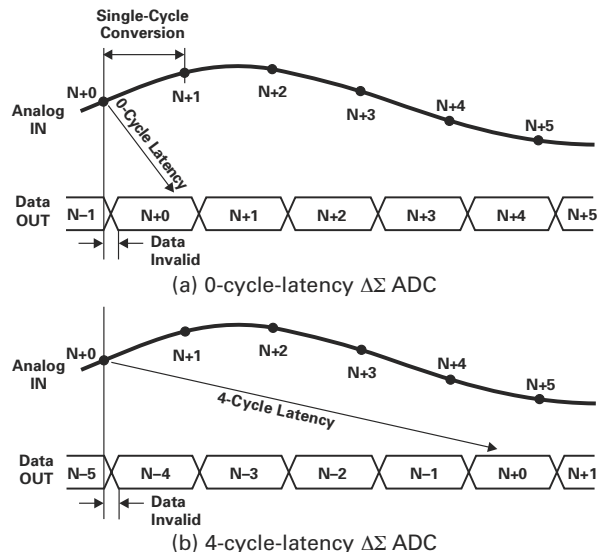


Figure 2: Cycle-Latency Comparison of Two $\Delta\Sigma$ ADCs



A $\Delta\Sigma$ converter with zero latency will continue to acquire input samples during the sampling period and continually modulate the signal into a noise-shaped representation. The $\Delta\Sigma$ converter's digital low-pass/decimation filter accumulates the noise-shaped signal and generates the output code at the end of the N+0 period. A $\Delta\Sigma$ converter has zero latency if data is available before a new sampling period is initiated. The output code represents the oversampled, filtered-input signal. At N+1 the converter initiates the next sampling period.

In Figure 2(b), with 4-cycle latency, the sampling period of N+0 is initiated. The output data of N+0 is presented after the completion of four conversion cycles.

The successive approximation register (SAR) ADCs are capable of zero latency as are many $\Delta\Sigma$ converters. The better choice for the application shown in Figure 1 is a high-resolution, zero-latency $\Delta\Sigma$ ADC. Some data sheets for $\Delta\Sigma$ ADCs claim single-cycle conversions. This is another way of saying that a converter has zero latency.

Texas Instruments (TI) offers numerous multiplexed, zero-latency $\Delta\Sigma$ ADCs that provide low-noise, high-resolution solutions (see Figure 3). These $\Delta\Sigma$ converters are capable of masking the filter action and providing a fully settled signal at the end of one cycle. As an example, TI's 16-channel, 24-bit ADS1258 has an internal, fifth-order, sinc digital filter followed by a programmable, first-order averaging filter. When the converter is configured in its auto-scan mode, the cycle latency is zero. In the auto-scan mode, the ADS1258 scans through the selected channels automatically, with break-before-make switching.

ADC Model	0	1	2	3	4	5
MSP12xx ADS1216/7/8	✓	(✓)	(✓)	(✓)		
ADS1224 ADS1226	✓					
ADS1232 ADS1234	✓				(✓)	(✓)
ADS1240 ADS1241	✓					
ADS1242 ADS1243	✓					
ADS1256 ADS1258	✓					(✓)

(✓) Optional Mode of Operation

Figure 3. TI's Multiplexed Zero-Latency $\Delta\Sigma$ ADCs

ADC Latency Time

Latency time is typically viewed as the time required for an ideal step input to converge, within an error margin, to a final digital output value. This error band can be expressed as a predefined percentage of the total output-voltage step. The latency time of a conversion is the time between the beginning of the signal acquisition and the time when data is available to download from the converter. In contrast to the cycle-latency specification, the latency time (or settling time) is never equal to zero.

Figure 4 compares the latency-time performance of various multiplexed $\Delta\Sigma$ ADCs. The latency time of a zero-latency $\Delta\Sigma$ ADC varies from device to device, depending on the system clock and the order of the converter's digital filter. A requirement for larger applications is that the multiplexed ADC must quickly cycle through the channels. The latency time for these types of applications can be critical. When the ADS1258 is configured in its auto-scan mode (zero latency), the output data is fully settled at the end of each conversion. The minimum latency time in the ADS1258's auto-scan mode is 42 μ s.

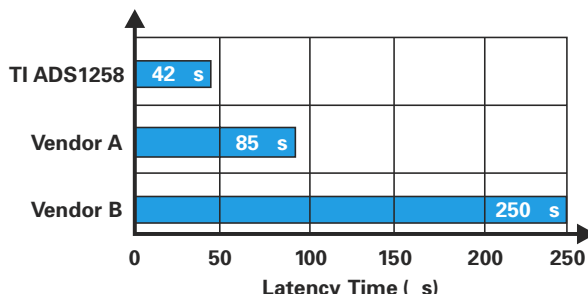


Figure 4. Latency-Time Comparison of $\Delta\Sigma$ ADCs

It is possible to reduce the throughput time of a zero-latency $\Delta\Sigma$ ADC if the intermediate or masked digital filter results are available. In this mode, the digital output results are not necessarily fully settled. For these devices the throughput time is always less than the latency time. Reduction of throughput time best suits sensors that produce small voltage changes at a slow rate (such as temperature sensors, pressure sensors, or load cells). With these types of sensors it might be advantageous to acquire several conversions and perform post-processing on the data.

When the ADS1258 is configured in its fixed-channel mode, the intermediate results from the fifth-order digital filter are available to the user. In the ADS1258 fixed-channel mode, the converter is no longer automatically cycling from channel to channel, and the output data may or may not be fully settled. The minimum throughput time of the ADS1258 in fixed-channel mode is 8 μ s (1/5 of the fully settled latency time).

Conclusion

The economy and efficiency of using multiplexed $\Delta\Sigma$ ADCs for applications with multiple sensors must be weighed against possible problems caused by ADC conversion latency and any latency introduced by external processing. The TI ADS1258 offers 16-channel, 24-bit conversions with low noise and zero latency. The device's single-cycle, low-latency-time capability provides fully settled data at the end of each conversion cycle. In auto-scan mode, the ADS1258 can complete conversion of all 16 channels in under 700 μ s. Cycle latency and the total conversion time must be evaluated for each ADC considered to be sure the device will perform as intended.

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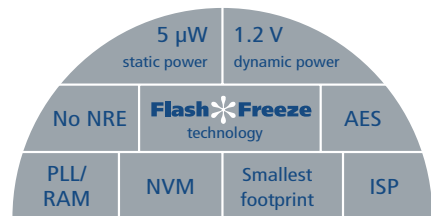


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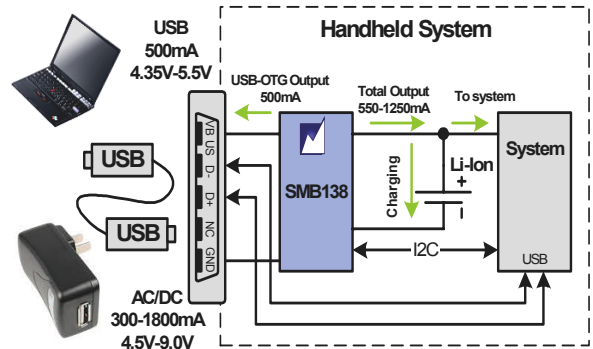
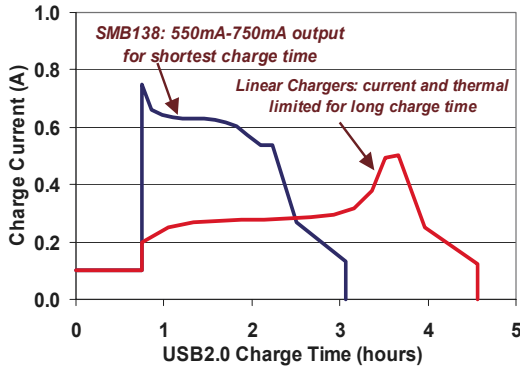
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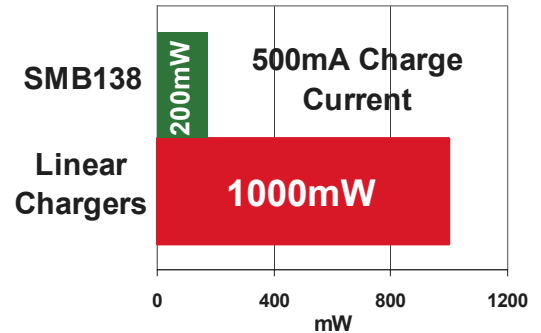
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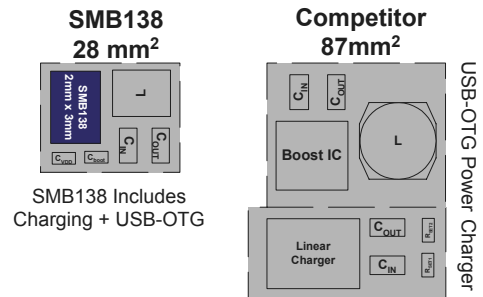


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Driving a dc solenoid as a control-loop element can be difficult, even though a solenoid is a simple device. Many applications require the solenoid to engage several times a second, especially if the control loop is regulating a fluid's rate of flow from a valve.

The use of digital logic can tempt you to try to drive a solenoid as though it were a relay—from a logic-device output via a transistor—but, in some applications, this approach is a mistake. Such power sources as batteries need voltage head room to supply current to the solenoid while powering the rest of the system. Even if the solenoid's average power is low, the peak current drawn from the battery, especially near the end of its life, can create a brownout condition. Conversely, if the voltage is high, the current through the solenoid coil can heat the device to the point of malfunction.

Some of the problems you might experience from this type of circuit are dropout conditions, in which the solenoid fails to engage, and long turn-on and turn-off times. If the solenoid is in a control loop, the loop could become unstable and destroy the solenoid. Few things smell worse than burning magnet wire and varnish. If it must be part of a control loop, a solenoid nearly always requires a carefully chosen method of active-current control.

As an electrical load, a solenoid behaves as an air-core inductor. In essence, a solenoid consists of magnet wire wrapped around a plastic, ceramic, or brass bobbin with a ferrous case (**Figure 1**). The case contains the magnetic field that you generate when you drive current through the solenoid coil. A plunger made of ferrous material completes the magnetic path. The bobbin can also serve as a bearing for the plunger. As the air gap between the plunger and the case decreases, the magnetic field gets stronger, and the force that the plunger exerts on the load increases. Once you've completely seated the plunger in the bobbin, its top and bottom close the air gap. The magnetic field flows through the top of the plunger and out the bottom. At first, the solenoid's inductance is high because of the large air gap. Because a magnetic field flows through iron more easily than it flows through air, the coil needs the most current initially to generate a field strong enough to actuate the plunger. The required initial current is the turn-on, or pull-in, current. Once the magnetic field is shorted through the case and the plunger, a smaller current—the hold current—can keep the solenoid closed, because the ferrous case and plunger carry the magnetic field.

An electromechanical relay is a reactive device you use to

actuate a switch. Electronically, relays and solenoids are similar, because you can treat both as inductors, but the similarity ends there. A solenoid resembles a motor more than it does a relay. You use solenoids, like motors, to convert energy from one form to another—usually electrical power to mechanical motion. Solenoid motion can be rotational or linear but is typically unidirectional with a return spring bringing the plunger or arm back from the actuated position. Some solenoids operate bidirectionally, but they require two drive circuits. You must limit the on-time of most solenoids because of damage that can occur from heating of the wire. One way to limit heating is to reduce the voltage across the coil after you've actuated the solenoid and closed the air gap.

Figure 2 shows a solenoid as the control element in a feedback loop. The controller sends commands to actuate the solenoid, which controls a process. In this example, the solenoid gates fuel a thruster valve. Solenoids open the valves; springs close them. The requirements for the solenoids specify opening and closing times, maximum and minimum on-times, duty cycle, and repeatability. The example reviews two control methods: open and closed loop. At first glance, it was tempting to use a transistor array to drive the solenoid from a logic device in an open voltage loop. If you had a stable power source for the drive, an open-loop voltage-switching transistor array might work. A stable power source is not the only factor

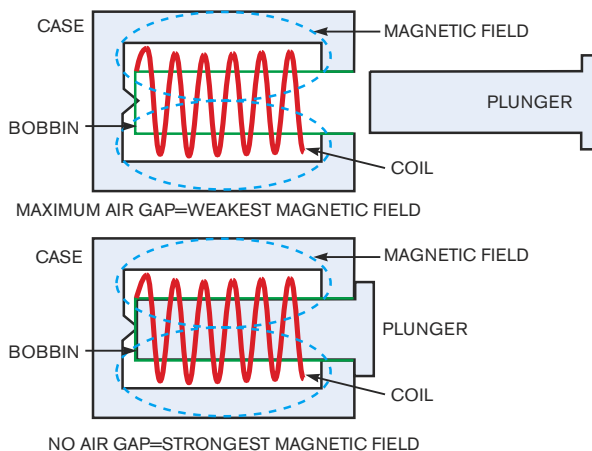


Figure 1 In essence, a solenoid consists of magnet wire wrapped around a plastic, ceramic, or brass bobbin with a ferrous case.

that determines the control method, however. Variability in the solenoid's operation can cause problems. On- and off-times become dependent on voltage changes and on the solenoid's dc resistance. In this example, the power source is a thermal battery that exhibits voltage decay as great as 10V. In the open-loop configuration, you must specify the solenoid's operation at the minimum voltage level—when the battery nears the end of its functional capacity. A closed current loop requires more components, and the loop's behavior must not interfere with the process controller's performance. Before you can select a control method, you must thoroughly understand the solenoid's load characteristics and the operational parameters of the process under control.

You can treat solenoids in a driven load as inductors. However, you must consider some solenoid characteristics when you size your power source and drive circuits. Solenoids are built not for a specific inductance value, but to achieve torque. As a solenoid actuates, its inductance changes. So, during operation, the electrical load behaves as if it were a variable inductor. The amount of torque that the solenoid can generate depends on the strength of the magnetic field. Field strength relates to the current in the coil and the number of turns of wire on the bobbin. If you need more torque, you need either more current or more turns of wire. The coil inductance and the dc resistance of the wire wound around the bobbin limit the solenoid current. The solenoids in this application were small but had an initial inductance of 3.3 mH and a dc resistance of 15Ω. To get the torque required to overcome the spring and open the valve, the driver had to supply 2.2A for 5 msec at pull-in and 0.75A to hold for as long as 2 sec. After this current-versus-time profile, the solenoid had to be able to respond again within 20 msec. According to Ohm's Law, the driver had to supply at least 33V to the coil during turn-on and 11.25V to hold.

Initially, it appeared that voltage control might be appropriate, but there were some other issues to consider. As current flows through the coil, the wire becomes warmer and its resistance increases—an effect known as I^2 loss. The gauge of the wire in the coil determines how much self-heating occurs. The thermal mass of the solenoid helps to dissipate the heat, but the turn-off time of only 20 msec does not allow for much dissipation. These solenoids were wrapped with approximately 435 in. of #36 AWG magnet wire. The following equation predicts the coil's self-heating as an algebraic adaptation of the fusing-current equation: $T = T_A + 10^{(33S(I/A)^2 - 1) \times (234 + T_A)}$, where S is the application time in seconds, T is the end temperature of the wire after S seconds, A is the area in square mils of the conductor, I is the application current, and T_A is the ambient temperature (Reference 1). The equation for calculating the resistance of the wire is: $R_t = R_{20} \times [1 + a_{20} \times (t - 20)]$, where R_{20} is the resistance at 20°C, a_{20} is the temperature coef-

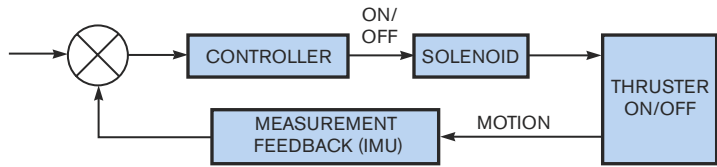


Figure 2 A solenoid is part of the feedforward path of this feedback-control system, which controls the delivery of fuel to a thruster valve.

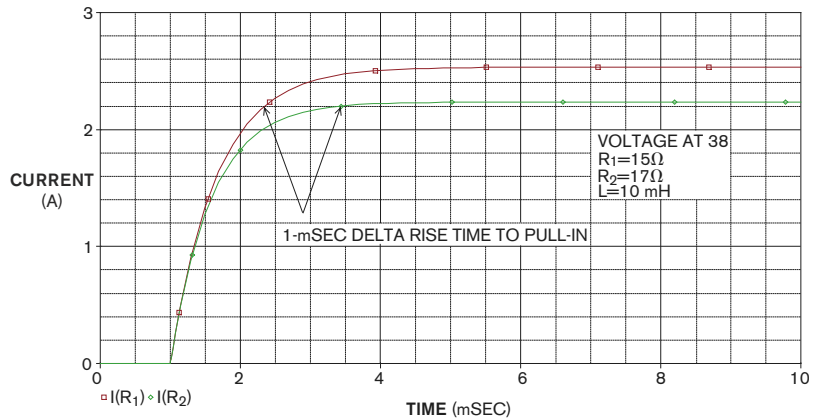


Figure 3 Thermally induced changes in dc resistance affect a solenoid's pull-in and release times. As the dc resistance changes, the charging-time constant also changes. This PSPICE plot shows the time-constant variation.

ficient of resistance for copper at 20°C=0.00393, and t is the end temperature (Reference 2).

Using these equations together and the earlier described current-versus-time profile, the coil resistance after the first cycle is 17.3Ω. The voltage required to achieve pull-in during the next pulse increases to 38.1V. The hold voltage increases to 13V. The increase in temperature does not include any soak back from the thruster itself, and normal variations in dc resistance are not associated with the coil winding. After a few more actuations, the solenoid heats up so much that it can no longer achieve the turn-on current. The result is that the fuel going to the thruster either is not properly regulated or simply fails to reach the thruster.

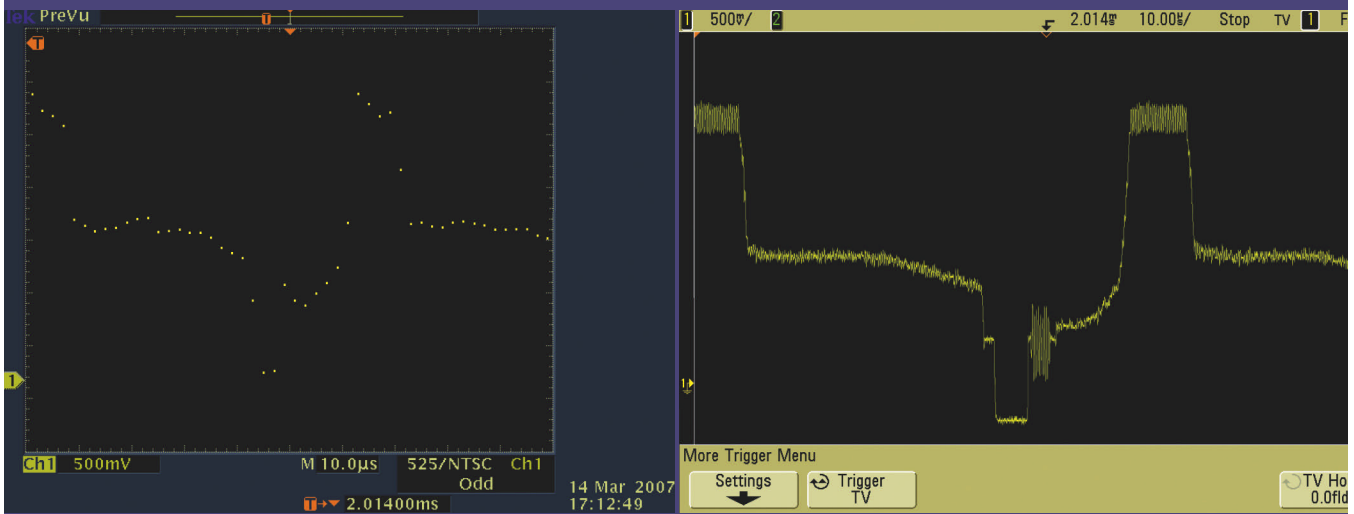
The change in dc resistance also affects the solenoid's pull-in and release times. As the dc resistance changes, the charging-time constant also changes. Figure 3, a PSPICE plot, shows the temperature-induced time-constant variation. The example uses a power supply of 38V so that both inductors could reach a current of 2.2A. The plot clearly shows a 1-msec difference in the time to reach the turn-on current. The solenoid does not actuate until the device has reached the turn-on current.

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 *Tektronix TDS3000B Series User Manual 071-0957-04, October 4, 2004.
 **Agilent 5000 Series Oscilloscope data sheet, Pub No 5989-6385EN, April 18, 2007.
 Agilent and Tektronix oscilloscope acquisitions taken at identical settings: horizontal timebase = 2ms/div, vertical volts/div = 500 mV/div, connect the dots = on. 10:1 passive probes used for both measurements. Final screen images show both acquisitions zoomed in to 10 μs/div.



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noid, the longer it takes to achieve the turn-on current, the hotter the wire gets, and the hotter the wire, the larger the dc resistance. Controlling the voltage across the solenoid does not help. Changes in dc resistance over time affect the solenoid's actuation time. Because an inductor is a current-dependent device—that is, the voltage across it is proportional to the first derivative of the current through it—controlling the current in the coil is the better choice. In this application, all of the variables associated with the solenoid's behavior make it challenging if not impossible to achieve consistent operation in an open loop. Closed-loop control is obviously necessary.

Controlling the voltage makes no sense. Because an inductor is a current-dependent device, you must control the current in the inductor. Doing so can ensure reliable operation. Update the control loop of **Figure 2** to add a current loop in the solenoid-control-element box (**Figure 4**). The elements of the current loop are the solenoid coil, the PWM (pulse-width modulator), and the feedback amplifier. The controller is an on/off-type element that may supply fuel to the thruster. The current loop is inside or nested in the fuel-command-control loop. The process loop establishes the requirements for the current loop. A complete understanding of the process loop's functional requirements is critical to properly designing the current loop. This example uses a 50-Hz process-control loop. That is, update commands from the controller to the solenoid-control element occur every 20 msec. To fully meet the thruster demand before the controller's next command, the solenoid-

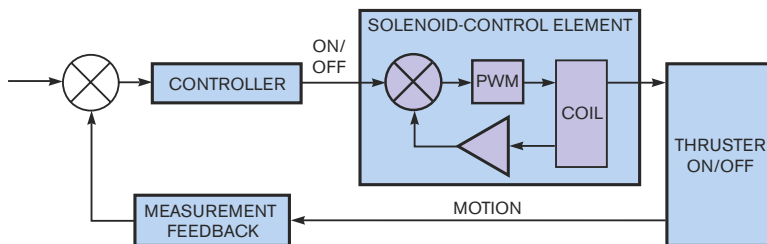


Figure 4 The elements of the current loop are the solenoid coil, the PWM (pulse-width modulator), and the feedback amplifier. The controller is an on/off-type element, which may supply fuel to the thruster. The current loop is inside or nested in the fuel-command-control loop.

control element must respond to the commands in much less time than the reciprocal of the update rate. The current loop's frequency response must be much faster than that of the process loop; a bandwidth of at least five to 10 times that of the outer loop is a good rule of thumb, because it ensures that the solenoid loop does not create instability in the outer loop. Therefore, a bandwidth of 1 kHz should work.

SYNCHRONIZE WITH THE SYSTEM CLOCK

Figure 5 shows the solenoid-control-element and the control-signal-timing relationships. The PWM-clock frequency must be high enough to establish the resolution of the drive current. Fortunately, the solenoid is a binary device; it is either on (2.2A) or off (0A). The circuit's two control points are turn-on (2.2A) and hold (0.75A). If the solenoid is part of

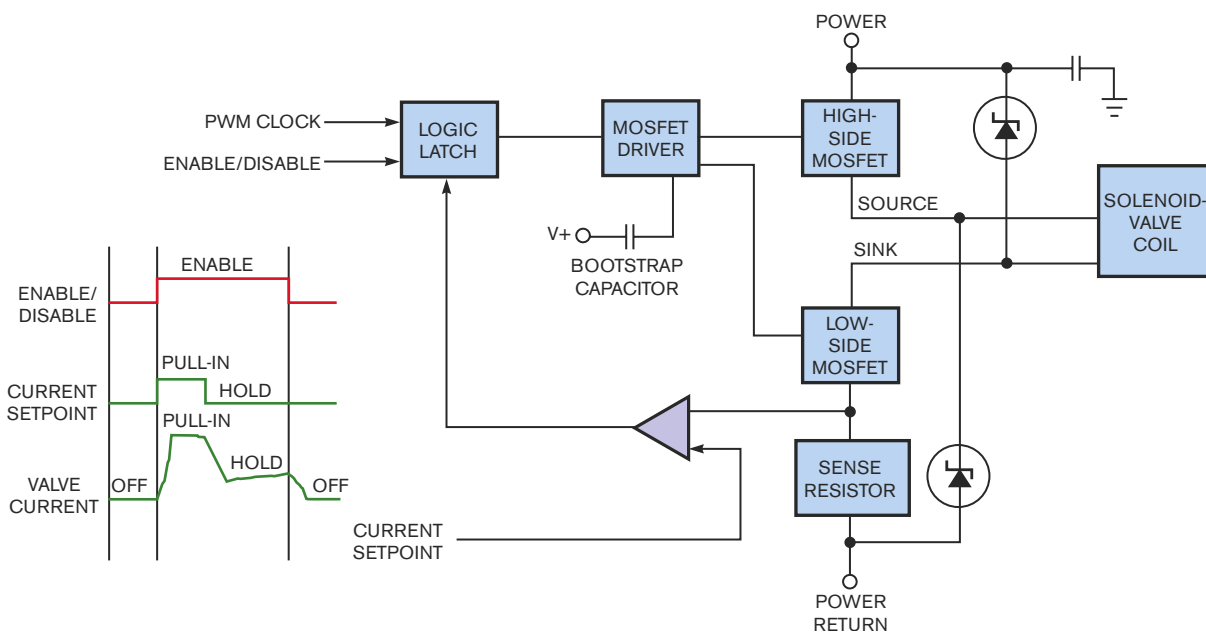


Figure 5 In the solenoid-control-element and control-signal relationships, the PWM-clock frequency must be high enough to establish the resolution of the drive current.

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At the Heart of Innovation

noise from adversely affecting the rest of the system is to limit the paths from the switcher to any victim circuits that may be near. Experts have written volumes on the layout and routing of charge-coupled amplifiers (Reference 3). The amount of analysis depends on the noise susceptibility of the rest of the system. Some good ground rules are to keep the length of the traces from the MOSFETs to the capacitor and diodes as short as possible and to install resistors in series with the MOSFET gates to slow the switching transitions. Even a 0Ω resistor affords the opportunity to change the bandwidth at the MOSFET gate.

It is critical that the routing plane have a heavy ground plane no more than one dielectric layer away. The source and sink traces must be very wide, and it's best to route them on top of each other all the way to the connector. From the connector to the solenoid, use shielded, twisted-pair wire. When you compute the load resistance, remember to include the IR drop across the harness. Keeping the noise down in a circuit is about controlling current loops. Make sure to route the solenoid current using a low-impedance path of minimum length.

A solenoid is an inductive load. Inductors are current-controlled devices. The best method for driving a solenoid is a current-control loop. However, current-loop controllers take up more space in a design because of the increased component count. If there is enough board real estate, a current loop is

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the only way to go to get precise control over the solenoid. Incorporating as much of the loop into programmable logic is a way to reduce the number of components. The needs of the system dictate the type of control to use. The controller presented here is simple and consumes approximately 2 in.² of board area. More current requires more area. When precise solenoid operation is less important than board area, open-loop voltage control can work. **EDN**

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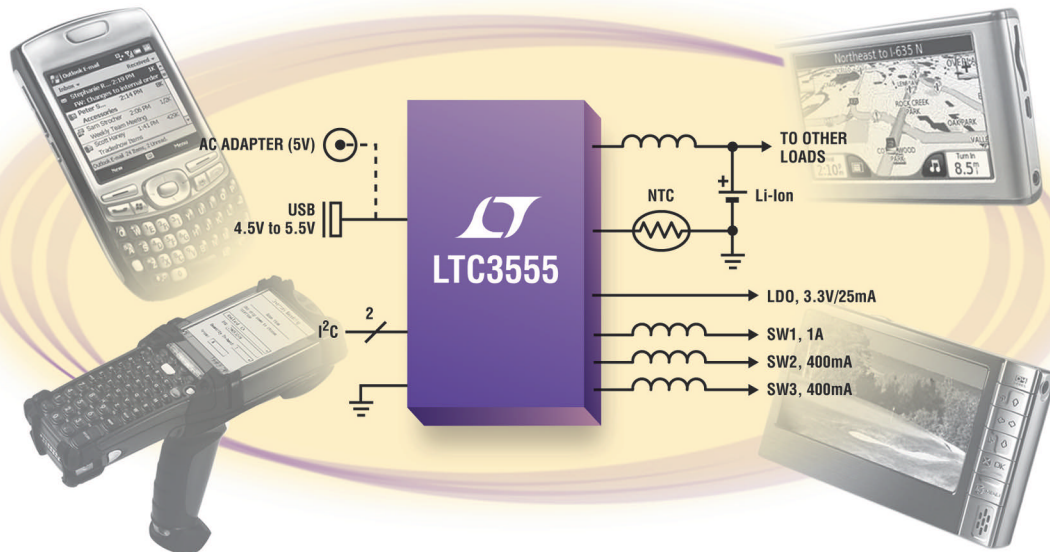
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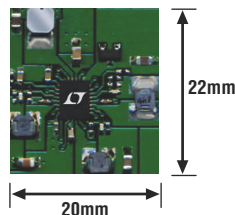
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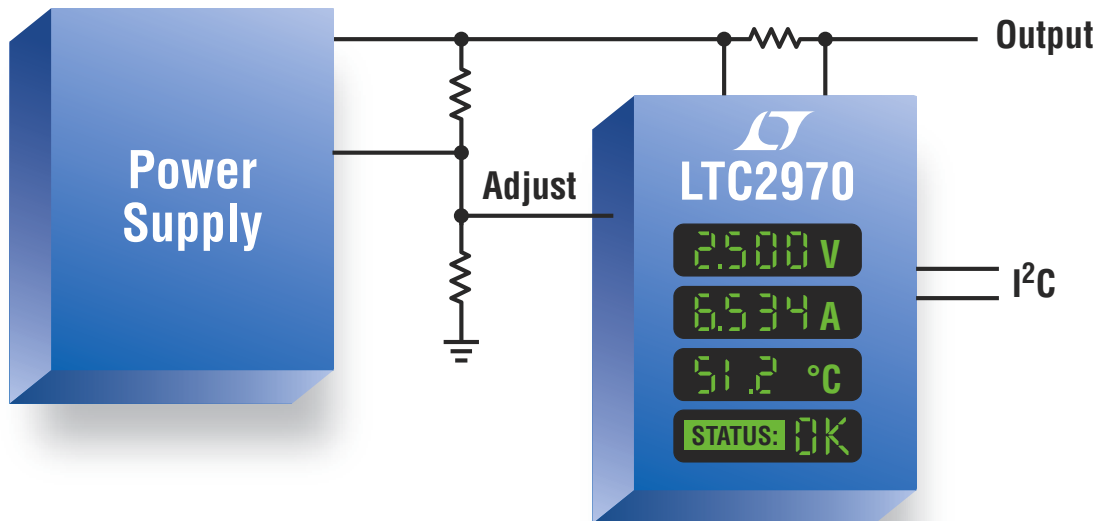
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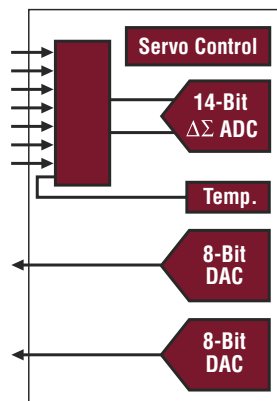
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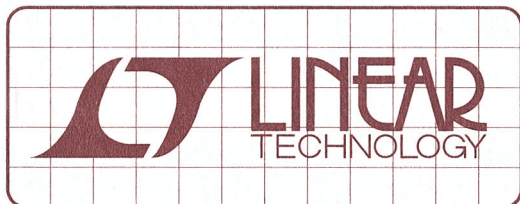
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DESIGN NOTES

An Easy Way to Add Auxiliary Control Functions to Hot Swap Cards – Design Note 421

Mark Thoren

Introduction

A Hot Swap™ controller is essential to any system in which boards are inserted into a live backplane. The controller must gently ramp up the supply voltage and current into the card's bypass capacitors, thus minimizing disturbances on the backplane and to other cards. Likewise, it must disconnect a faulty card from the backplane if it draws too much current. The controller also monitors undervoltage and overvoltage conditions on the backplane supply, ensuring reliable operation of the card's circuitry. The LTC4215-1 takes the obvious next step and integrates three general purpose I/O (GPIO) lines and an accurate ADC into the Hot Swap controller to provide quantitative information on board voltage and current. Upgrading to the LTC4215-1 is analogous to replacing a car's venerable "Check Engine" light with a modern dashboard information display.

Additional Control

There are many functions on a card that are considered part of the "power gateway," apart from the actual function of the board (telecommunications, data acquisition, etc.) These include sequencing power supplies, providing supply status information, monitoring pushbuttons, etc. The LTC4215-1 GPIO pins are well suited to these functions. Tying the ON pin high turns on the pass FET after a 100ms power-on delay. Grounding the ON pin enables software control of the FET. The state of the GPIO pins can be set before enabling the FET, ensuring a known state when downstream power is enabled. GPIO1 defaults high on power up, and can sink 5mA. GPIO2 defaults high and can sink 3mA. GPIO3 defaults low and can sink 100µA.

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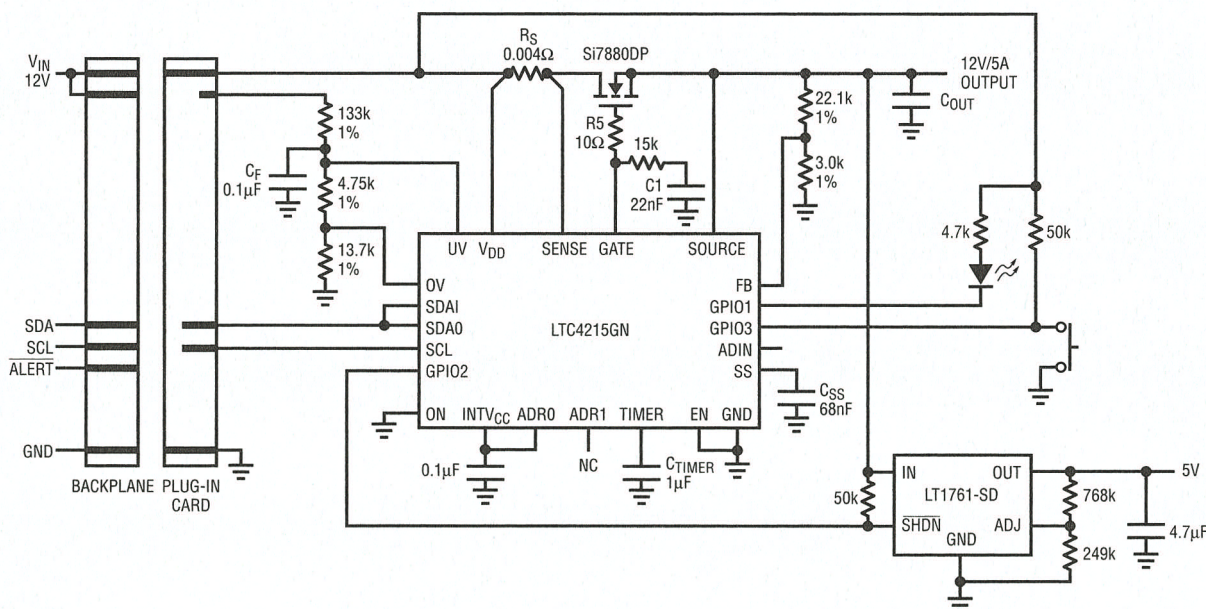


Figure 1. The LTC4215-1 in a Typical Card Resident Application

For instance, Figure 1 shows an application that monitors a “request to remove card” pushbutton and lights an “okay to remove” LED when the card is ready for removal. This permits graceful shutdown of the card. For example, it can transfer collected data before shutting down so that it is not lost. GPIO1, which defaults high, controls the LED. GPIO3 is reprogrammed as an input that monitors the state of the pushbutton. The GPIO2 pin controls the operation of an onboard regulator. This is important in mixed signal circuits, where analog circuitry may need to be powered up before digital signals are enabled.

Figure 2 uses a GPIO pin to control an LTC4210-1 Hot Swap controller, which in turn controls a 3.3V rail. Once again, this is useful for sequencing supplies and may eliminate the need for additional sequencing circuits.

Figure 3 uses all three GPIO pins to light one of eight LEDs using a 74HC138 decoder. These can indicate system status or power consumption. Other possible functions include issuing a microprocessor reset, adding additional channels to the ADC using the GPIO pins to control a multiplexer, or interfacing with an advanced power supply sequencer such as the LTC2928.

Conclusion

The LTC4215-1 is a smart power gateway for Hot Swap circuits. It provides fault isolation, closely monitors the health of the power path, and provides an unprecedented level of control over the inrush current profile. The three general purpose I/O pins and a spare ADC channel allow further control of power path and system initialization/shutdown related functions.

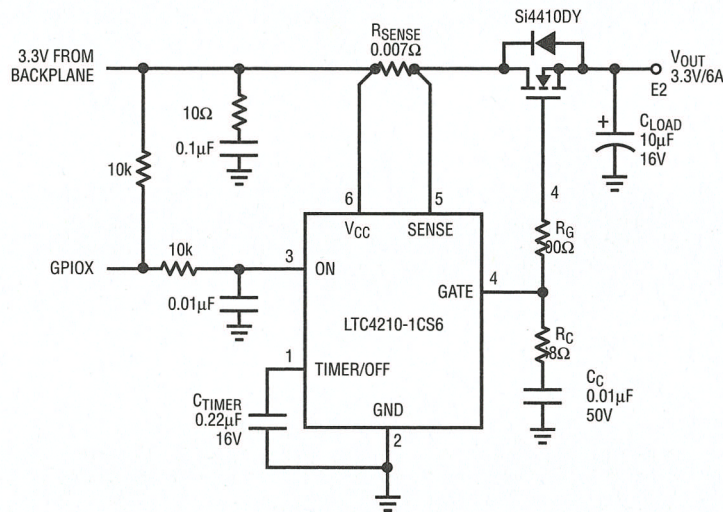


Figure 2. Controlling an LTC4210-1

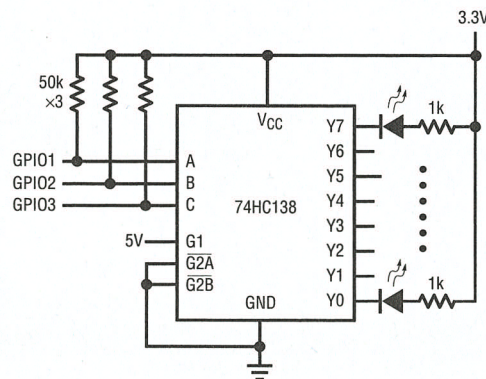


Figure 3. Controlling Eight Status LEDs

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Simple and effective inrush-current limiter stops surges

Gregory Mirsky, Juno Lighting Group, ModuLight Division, Des Plaines, IL

Offline power supplies that drive loads of 200W and more require inrush-current limiters. Unrestricted inrush currents can reach hundreds of amperes, which may damage the line rectifier, open the fuse and input-filter inductors, and damage the PFC (power-factor-correction) filter capacitors. A simple method of limiting the inrush current uses an NTC (negative-thermal-coefficient) thermistor that connects in series with the supply line. When cold, the thermistor presents a high resistance, but its resistance decreases significantly as its temperature increases, limiting the inrush current by virtue of its thermal inertia and inability to quickly decrease its resistance.

However, an NTC thermistor also presents some resistance to the power

supply's normal operating current. To keep the thermistor's normal resistance low, it should operate at a sustained and relatively high temperature, but this scenario may impair the power supply's temperature profile and raise the temperature in an enclosure in which power dissipation is already substantial.

This Design Idea offers an alternative circuit that effectively limits inrush current and does not add an extra source of heat to the power-supply package. Without increasing power losses during normal operation, a switchable series resistor in the power supply's dc section can efficiently limit inrush current until the PFC-rail electrolytic capacitors acquire a full charge. Then, an electromechanical or optically isolated semiconductor relay short-circuits the resistor.

DI Inside

68 Inverting sample-and-hold amplifier requires no external resistors

70 Single IC forms inexpensive inductance tester

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However, determining whether the PFC capacitors are fully charged presents a problem. Universal power-supply designs operate over a range of ac-input voltages, and determining the voltage that indicates a full charge can thus prove elusive. In addition, the inrush-current limiter should delay operation of any internal auxiliary power supplies and other power-consuming circuits to allow the PFC-rail capacitors to charge to their full predetermined extent.

The easiest method of solving these

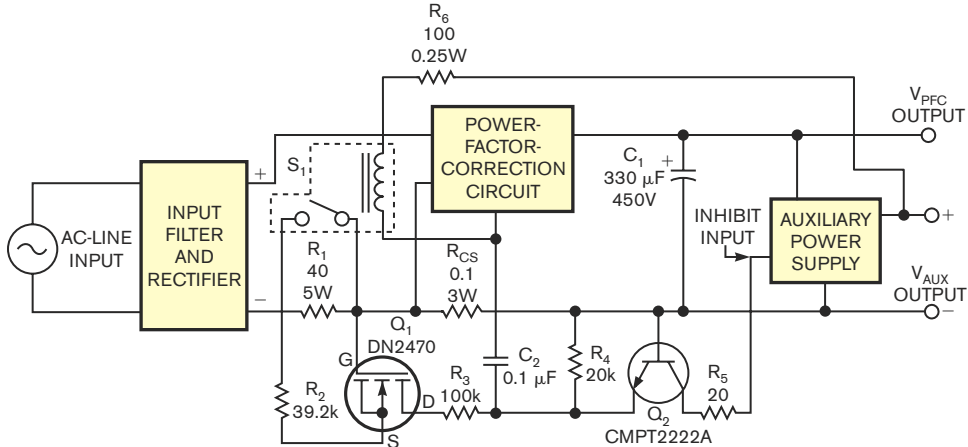


Figure 1 This inrush-current-limiter circuit features an electromechanical relay, S_1 , and a current-limiting resistor, R_1 . (Unless otherwise mentioned, all resistors in the schematic are rated for 0.125W.)

problems uses a circuit that measures the inrush current itself and not the voltage across the PFC capacitors. It determines the end of the inrush process by monitoring extinction of the inrush current's amplitude. Upon reaching a preset threshold, the circuit commands the start-up of auxiliary power supplies and other circuits. Monitoring the inrush current allows effective control of the power supply's starting point and renders the start-up threshold independent of the input-line voltage.

Figure 1 shows a practical version of a PFC circuit, which employs a switched-resistor inrush-current limiter. The inrush-current-sensing sub-circuit comprises a wirewound resistor, R_1 , and a parallel depletion-mode MOSFET, Q_1 , which connects to resistor R_2 as a current source that drives resistors R_3 and R_4 . Over a wide range of the voltage drop across R_1 , from a few hundred volts to a few volts, this circuit generates a small constant current that suppresses operation of the auxiliary power supply and prevents interference with the inrush-current-limiting process.

When the inrush current decreases sufficiently, the voltage drop across R_1 becomes insufficient to keep Q_1 in operation as a current source. Q_1 's current extinguishes, allowing the auxiliary power supply to turn on and start the power supply, by activating relay S_1 , whose contacts short-circuit R_1 . R_2 's value determines the current necessary to hold the auxiliary power supply in a disabled mode, allowing PFC-rail capacitor C_1 to charge fully.

A 12V electromechanical relay, such as Omron's (www.omron.com) G2RL-1, provides low-resistance contacts to bypass R_1 (Reference 1). As an alternative, an optically isolated solid-state relay, such as the Carlo Gavazzi (www.gavazzionline.com) RP1A48D5, with a MOSFET or an SCR (silicon-controlled-rectifier) output device can replace S_1 , provided that the voltage drop across the output device introduces no substantial power loss (Reference 2).

Figure 2 depicts the charging process's waveform as the voltage drop

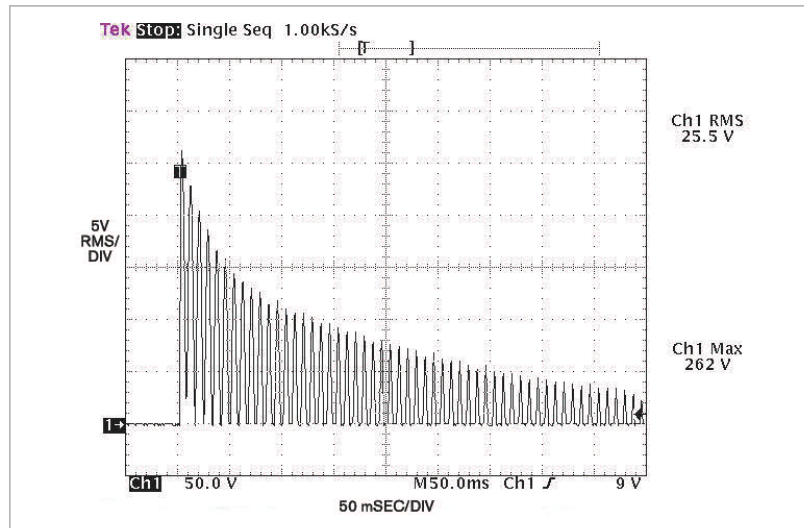


Figure 2 The voltage across the 40Ω current-limiting resistor, R_1 , exhibits a classic exponential decay as the power-factor-correction capacitor approaches a full charge; the auxiliary power supply is deactivated for clarity.

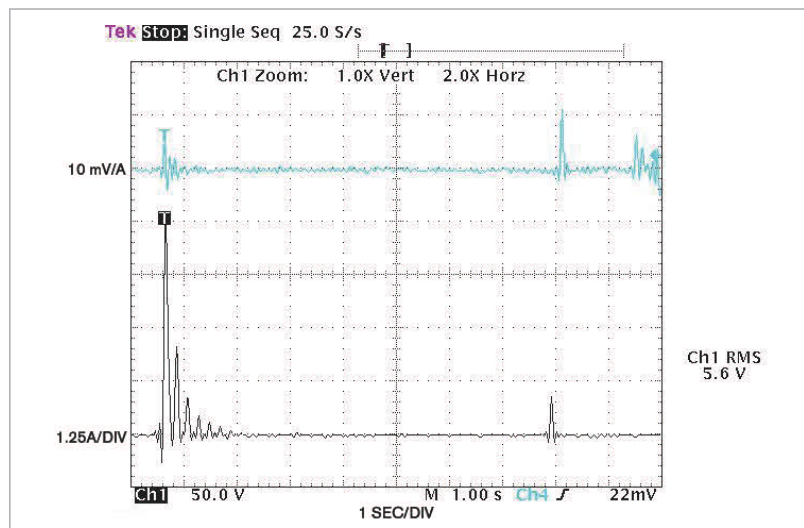


Figure 3 The upper trace shows the current as measured with a current probe. The lower trace depicts the voltage drop that the input current across resistor R_1 produces.

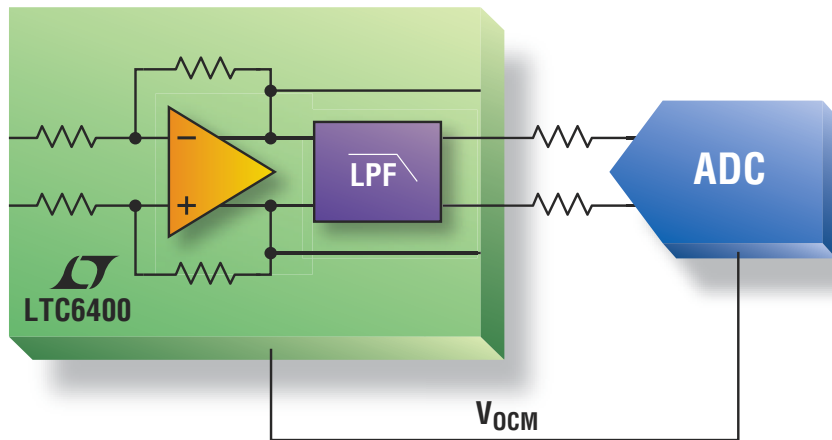
across R_1 . The exponential envelope and its subcycles represent components of the inrush process; R_3 and C_2 filter out the subcycles and produce a decreasing exponential voltage waveform across R_1 , holding Q_2 on for the duration of the inrush process. Q_2 suppresses the auxiliary power supply's operation by pulling its disable input low. At a few volts across R_1 , Q_1 stops generating constant current and shuts down Q_2 to enable the auxiliary power

supply. Thus, the entire power supply waits until the inrush current attains a safe value that R_2 sets. The power supply starts immediately after relay S_1 trips and shorts out inrush resistor R_1 . The remainder of Figure 1 comprises a conventional PFC but may also represent a part of any other power-supply configuration.

Trace 1 in Figure 3 depicts the start-up of a 2.4-kW power supply with the inrush-current limiter and a slow-start

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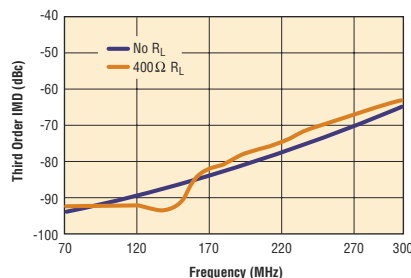
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circuit, which allows the separation of the inrush and the start-up processes. The inrush-current value is 5A, a relatively low value for a 2.4-kW power level. Trace 4 shows the input current measured with a current probe. **Figure 4** depicts a 2400W power-supply start-up. Its inrush current is intentionally approximately 5A, which is far less than its operating current of approximately 14A. **EDN**

REFERENCES

- 1 "PCB Relay, G2RL," Omron Corp, <http://ecb.omron.com.sg/pdf/relay/power/G2RL.pdf>.
- 2 "Solid State Relays PCB, 1-Phase ZS/IO Types RP1A, RP1B," Carlo Gavazzi, www.gavazzionline.com/pdf/rp1a48d5.pdf.

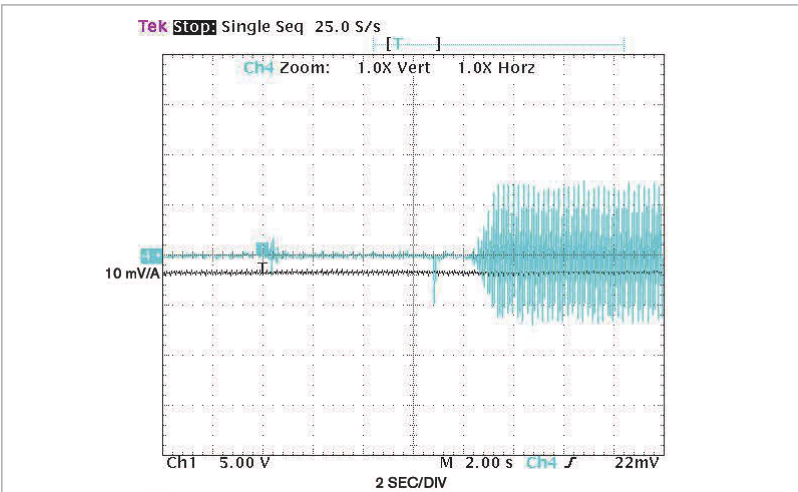


Figure 4 The input-current waveform shows the effects of the inrush-current limiter with the power supply driving a 2400W load.

Inverting sample-and-hold amplifier requires no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Many applications require a sampling circuit whose output is inverted with regard to the respective sample of an input signal. A

simple approach is a cascade of a common noninverting sample-and-hold amplifier and an inverting amplifier. A classic inverting amplifier is an op amp with voltage feedback from two resistors. The values of these resistors, which are usually equal, should be high enough to decrease the total power loss

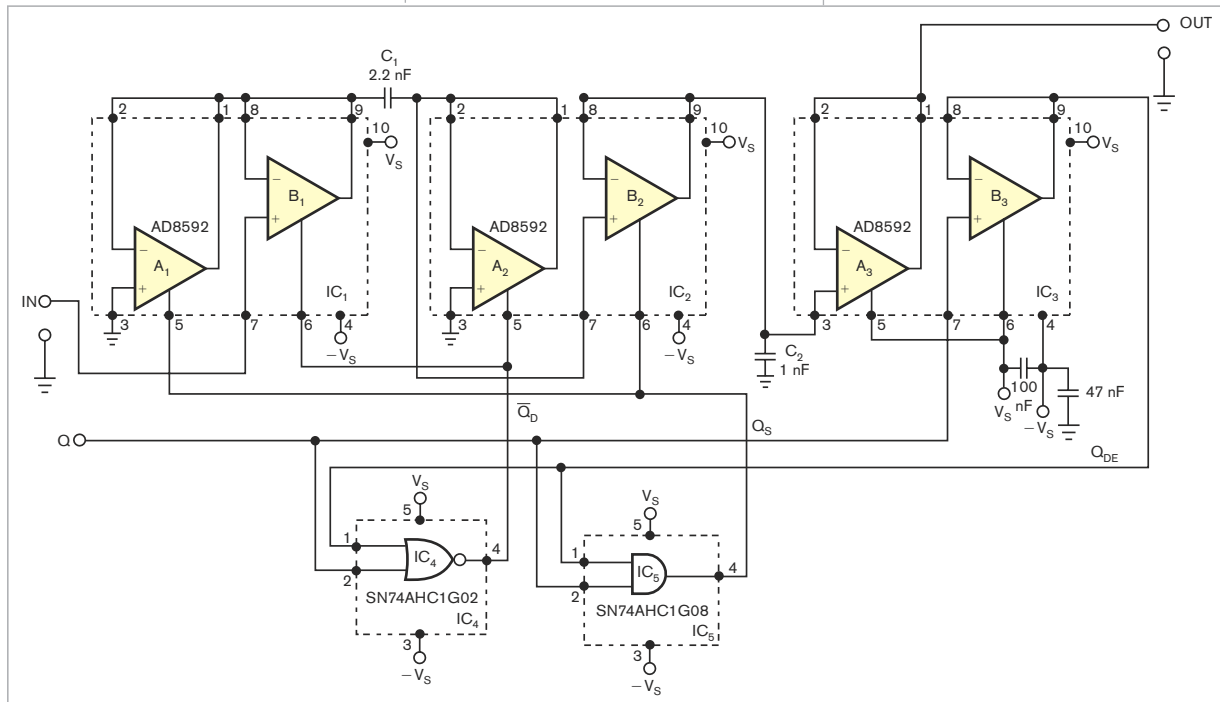
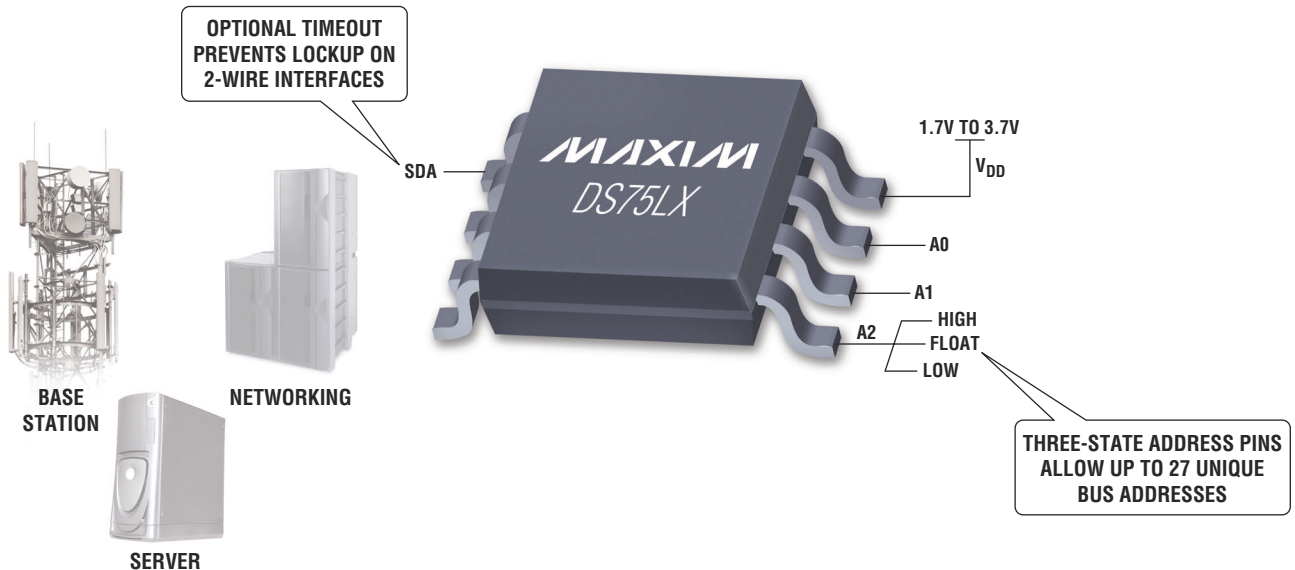


Figure 1 This sample-and-hold amplifier inverts the input signal by extension of its switched-mode circuitry.

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of $P=2V^2/R$, which is proportional to the square of the output voltage. The values of these resistors should be as low as possible to preserve the bandwidth of the op amp.

Any parasitic capacitance (C_2 in the following equation) parallel to feedback resistor R_2 forms a pole in the transfer function of the inverter. This pole results in an additional breakdown of the gain-frequency characteristic of the inverting amplifier, with the value of breakdown frequency of $f_2=(1/2\pi)\times(1/R_2C_2)$. To retain the widest possible bandwidth, $f_2>f_T$, where f_T is the transition frequency of the op amp—in other words, the frequency at which the open-loop gain of the op amp drops to unity.

The Analog Devices' (www.analog.com) AD8592 dual op amps, which have a high-quality shutdown function, allow you to use a different approach (Reference 1). The inverting sample-and-hold circuit in Figure 1 uses no external resistors. Thus, no power dissipates at external passive devices in the hold state of the circuit. All op amps act as voltage followers. In the hold state, followers B_1 and A_2 are enabled; thus, the B lead of the C_1 capacitor, Pin 1 of IC_2 , is grounded through the output of A_2 , and the input voltage, V_{IN} , gets followed at the A lead of the C_1 , Pin 9 of IC_1 . Upon the sampling command, Q is high, and, at this time, the A lead of C_1 gets

THE OP AMPS' HIGH OUTPUT CURRENT OF 250 mA CONTRIBUTES FURTHER TO THE FAST CHARGING OF CAPACITORS C_1 AND C_2 .

grounded through the output of the A_1 follower. This scenario causes a negative voltage of $-V_S$ to appear at the input of the B_2 voltage follower, which in turn charges the C_2 capacitor to the voltage of $-V_S$ at the beginning of the sampling command. Voltage follower A_3 serves as an impedance converter.

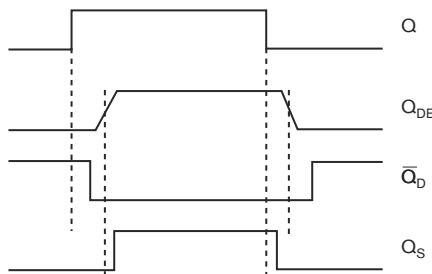


Figure 2 The external control-logic signal, Q, splits into two quasicomplementary signals to ensure the internal break-before-make operation of the sample-and-hold amplifier.

The AD8592's data sheet does not directly specify the leakage current at the output of the voltage follower; however, you can estimate it as being lower than 10 pA. Capacitors C_1 and C_2 thus can have unusually low values. On the other hand, the op amps' high output current of 250 mA contributes further to the fast charging of capacitors C_1 and C_2 .

The B_3 voltage follower serves as a delay line, which, in conjunction with one AND gate and one NOR gate, generates two semicomplementary logic-control signals (Figure 2). Both of these signals, Q_S and \bar{Q}_D , are thus kept at an inactive low level for a sufficiently long time, before moving to an active high level, providing a break-before-make operation. The input voltage gets tracked at the C_1 capacitor with \bar{Q}_D high, and the last value of this voltage, at the high-to-low transition of Q_D , is a sample. The sample, at the instant of the low-to-high transition of Q_S , appears with a negative sign at capacitor C_2 and subsequently at the output. **EDN**

REFERENCE

1 AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ± 250 mA Output Current and a Power-Saving Shutdown Mode, Analog Devices Inc, 1999, www.analog.com/zh/prod/0,1,759_786_AD8592,00.html.

Single IC forms inexpensive inductance tester

Luca Bruno, ITIS HenseMBERGER Monza, Lissone, Italy

This Design Idea shows how to build a reliable, low-cost, and simple inductance tester. The basis for the tester is a Pierce buffered CMOS oscillator (Figure 1). Instead of using the usual quartz crystal, you connect the inductor under test. This oscillator uses a single CMOS inverter bi-

ased through resistor R_1 in its linear region to form a high-gain inverting amplifier. Because of its high gain, the inverter dissipates lower power than an unbuffered gate; even a small signal drives the output high and low.

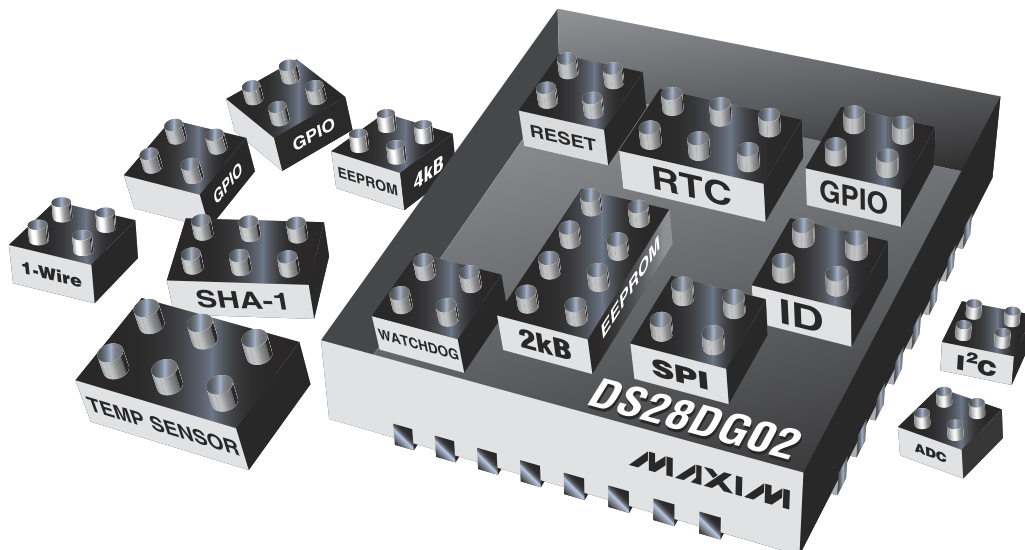
The $LC\pi$ network forms a parallel resonator that ideally resonates

at the frequency $f_0=1/2\pi\sqrt{L_X C_S}$, which corresponds to a period, T_0 , of $2\pi\sqrt{L_X C_S}$, where $C_S=C_1||C_2=50$ nF. So, you can calculate the inductance, L_X , by measuring the resonant frequency, f_0 , or the period, T_0 . At the resonant frequency, the $LC\pi$ network provides a 180° phase shift from input to output. To oscillate, the phase shift at frequency f_0 around the oscillator loop must be 360° , and the gain of the oscillator loop must be greater than one. Inverter IC_{1A} provides an addi-

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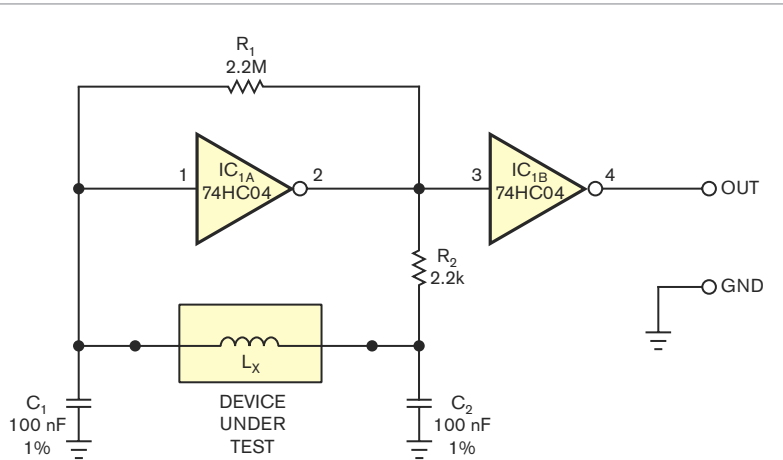
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tional 180° phase shift from input to output and a high gain to compensate for the attenuation of the network.

Resistor R_1 is not critical, and its value can be 1 to 10 M Ω . Resistor R_2 isolates the output of gate IC_{1A} from the LC π network so that you can obtain a nearly clean square wave from the output of the gate itself. In addition, R_2 improves frequency stability because it increases the slope of phase shift around the resonant frequency. For best performance, use film capacitors with low self-inductance, such as the MKP1837 polypropylene-film-capacitors series with 1% tolerance from Vishay (www.vishay.com). You can also use other film capacitors with standard tolerance provided that you select the value with a precision capacitance tester for best accuracy. The low supply current of the circuit allows you to use a battery as a power source. **EDN**



NOTES:
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Figure 1 Replacing a Pierce oscillator's crystal with an unknown inductance allows you to measure its value by observing the resulting oscillation's frequency.

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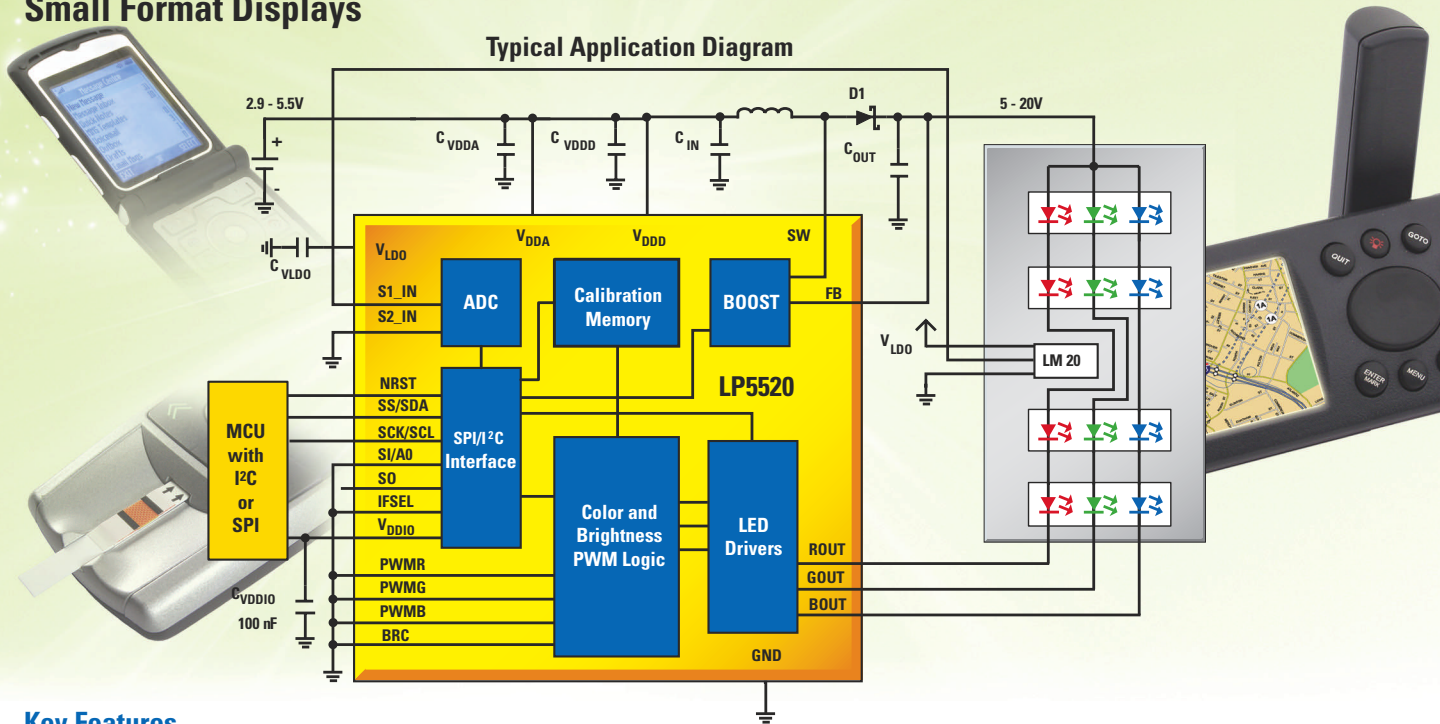
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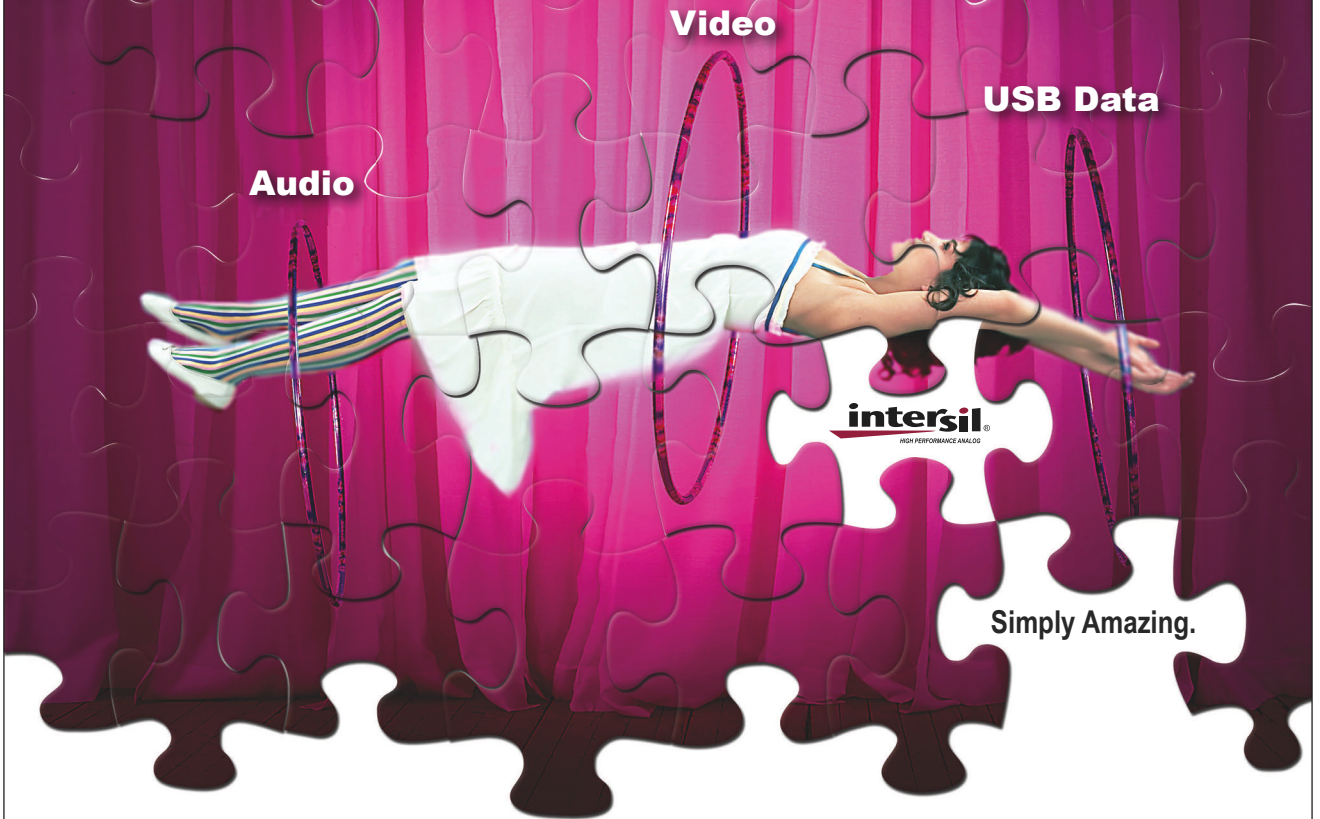
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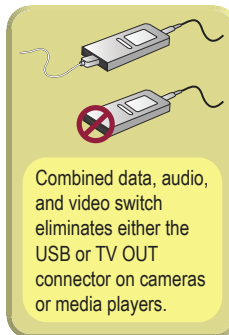
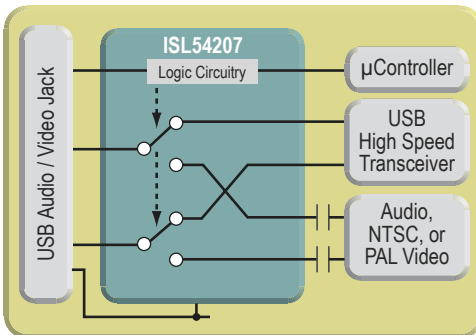
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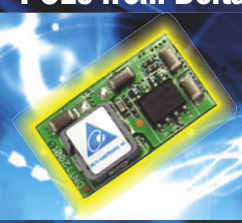
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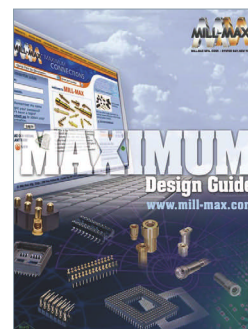
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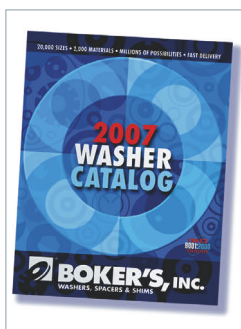
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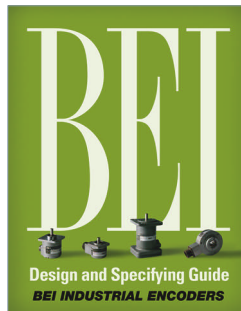
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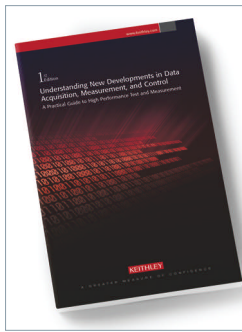


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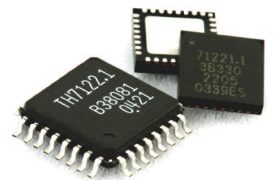
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LOOKING AHEAD

TO CONFERENCE SEASON

With the beginning of September, the August doldrums officially end and the conference season starts up again at full speed. High on the list for chip designers should be the IEEE Custom Integrated Circuits Conference, September 16 to 19 in San Jose, CA. The event offers technical sessions; a keynote by Texas Instruments guru Bill Krenick on the challenges of wireless design in advanced processes; and a panel discussion on the question of whether analog will fail to scale to 45 nm, leaving digital designers free to consume their analog brethren's lunches. Information is available at www.ieee-cicc.org/home.html.

LOOKING BACK

AT TROUBLE WITH ENGINEERING EDUCATION

Chief engineers are complaining about the poor educational grounding many recruits seem to have received for their work. "We get enough men to interview, but most of them are weak on fundamentals," one said. He continued that an engineer should have a good understanding of basic electronic circuits, particularly amplifier design and tube application. Some chiefs thought the problem was due to the volume

LOOKING AROUND

AT TODAY'S TROUBLE WITH ENGINEERING EDUCATION

Despite graduating huge numbers of engineers each year, India is reportedly facing such a shortage of qualified technical workers that some Indian companies are beginning to recruit senior people from the United States, and others are actually shifting operations to US technology centers such as Silicon Valley. Local costs in Bangalore, India, for hiring a senior programmer or design manager are reportedly approaching those in the United States, retention is nearly impossible, and a similar situation appears to be developing, more slowly, in China. Some of the problem is due to the enormous growth rates in the technology industries of both countries. But experts also cite problems with engineering and technical graduates, many of whom are simply not sufficiently grounded in the fundamentals to step into contributing roles in industry. The experts agree there is no quick answer, but something should be done.

of material engineering schools had to teach just to keep abreast of developments. Others suspected that since more engineers were graduating, their number naturally included more from the bottom quarter of the class. Perhaps emphasis should be shifted from advanced courses to fundamentals, or perhaps the curriculum should be lengthened. There's no quick answer, but something should be done.

—*Electrical Design News*,
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